

ADDENDUM
TO
INTECOLOR MAINTENANCE MANUAL
FOR THE
3800 & 8800 SERIES TERMINALS
999440-031 MAY 1988

This Addendum extends the Intecolor Maintenance Manual for the 8800 & 3800 Series Terminals to include terminals manufactured with wire frame construction and patented autoranging power supplies installed. All 3800/8800 series terminals share the same digital logic circuitry. The components of the optional graphics board were physically rearranged to allow for installation of a cooling fan. The analog circuitry of these wire frame terminals differs from that described in the existing manual. This Addendum is dedicated to the modular analog circuitry of these units.

This Addendum covers the following products:

3815	8814	8825
3825	8815	8826
3865	8816	8865
3875	8824	8875

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WARNING!

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FCC INFORMATION

This equipment generates and can radiate radio-frequency energy which may cause interference to radio communications. The 3800/8800 terminals have been tested and found to comply with the limits established by FCC Rules, Part 15, Subpart J, for Class A computing devices. These limits may not be wholly effective in preventing interference in particular installations. In the event of interference, the user shall be responsible for taking corrective action as required.

The Federal Communications Commission has prepared a pamphlet which addresses the problem of interference to commercial broadcast reception. The publication is available through the U.S. Government Printing Office, Washington, DC 20402. Request stock number 004-000-00345-4, How to Identify and Resolve Radio/TV Interference problems.

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SAFETY SUMMARY

This information defines WARNINGS and CAUTIONS statements. Specific warnings and cautions will also be found throughout the manual where they apply. Some general safety practices are also listed as a reminder to service personnel.

CAUTION statements identify conditions or practices that could result in damage to the equipment or property.

WARNING statements identify conditions or practices that could cause personal injury or loss of life

Power Source

The products discussed in this manual are designed to draw power from a single phase power source. The maximum voltage applied should not exceed 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection is required for safe operation.

Grounding the product

The ground conductor of the power cord provides the ground for this product. Plug the power cord into a properly wired (grounded) receptacle to avoid electrical shock.

Danger: loss of ground

With out the proper ground, all accessible conductive parts may provide an electrical shock. Knobs and controls, even the cover of a unit may be "energized".

Use only a power cord and/or connector that is in good condition and is specified for your product.

Use the correct fuse.

Using a fuse other than the one specified for the product may create a fire hazard. The replacement fuse must be identical in type, voltage rating and current rating.

Do not operate in explosive atmosphere, unless it has been specifically certified for such operation.

Internal circuitry could provide a spark or enough heat to ignite an explosion.

Do not service alone.

Service technicians should not work on internal circuitry alone. Another person capable of providing first aid should be present.

Do not wear Jewelry, or other conductive items that may come into contact with dangerous voltages and currents.

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19" CRT Terminals

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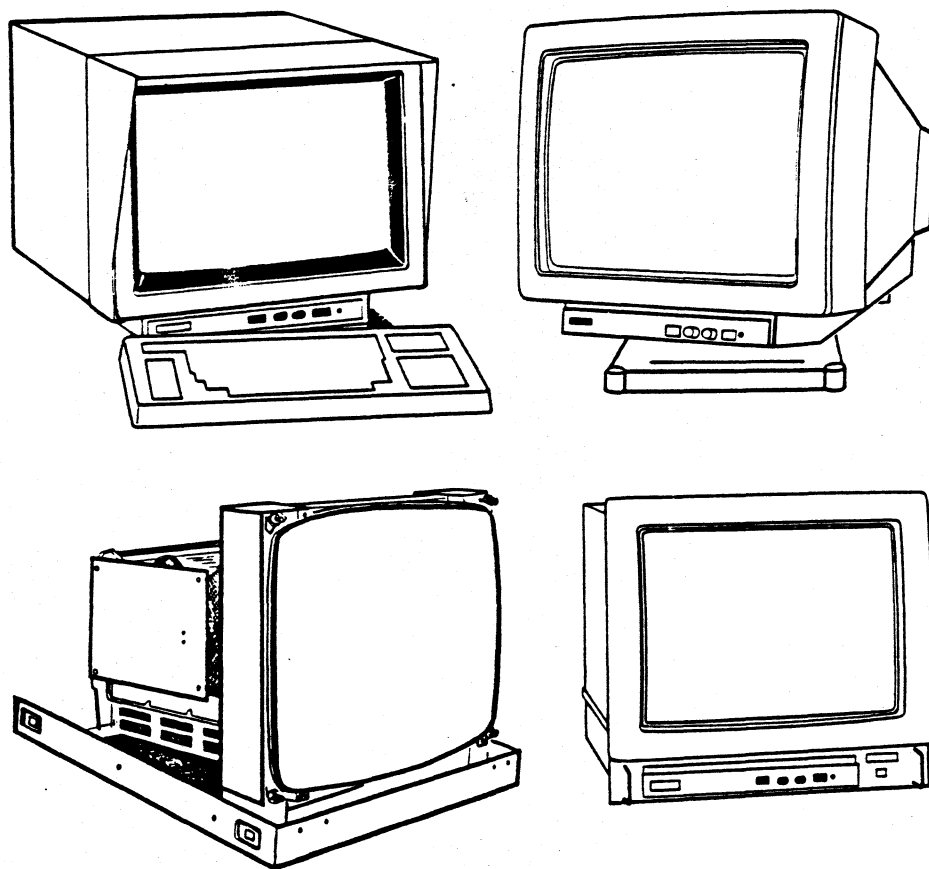
CHAPTER I

INTRODUCTION

CHAPTER I

INTRODUCTION

Improvements in Intecolor analog circuitry led to the development of new products for the 3800/8800 Series color graphics terminals. The analog systems described in this addendum feature Intecolor's patented Auto-ranging Power Supplies, and improved deflection and video circuitry.



All 3800/8800 Series terminals provide color alphanumeric displays on an 80 X 48 character grid. In addition, two levels of graphics resolution are available for all 3800/8800 Series terminals.

Graphics Grid:

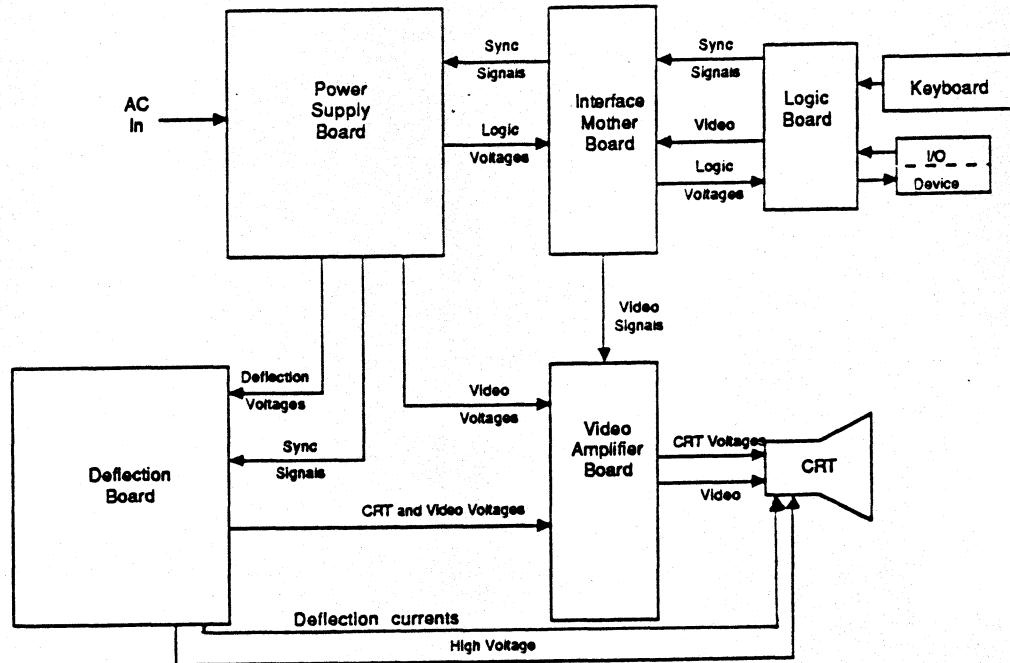
Normal Resolution	160 wide X 192 high
Medium Resolution	480 wide X 384 high

Screen size, monitor cabinet, graphics capabilities and analog circuitry used, determine the model number for each unit. See the chart in appendix A, for the available models of 3800/8800 Series terminals.

SYSTEM OVERVIEW

Three analog printed circuit boards, an interface/mother board, the logic board, and a pre-converged color CRT are included in basic 3800/8800 units described in this addendum. Units with extended graphics capabilities also use an additional logic board.

A system block diagram of 3800/8800 Series terminals described in this Addendum is shown below.



Power Supply circuitry converts input AC voltage into the many DC voltages required by other circuitry of the terminal.

Deflection circuits develop linear sawtooth currents to move an electron beam, synchronized with the logic, across the CRT screen. The high anode voltage and other CRT biasing voltages are also generated by deflection circuitry.

Video circuitry amplifies the one bit video signals from the logic to drive the CRT red, green, and blue cathodes.

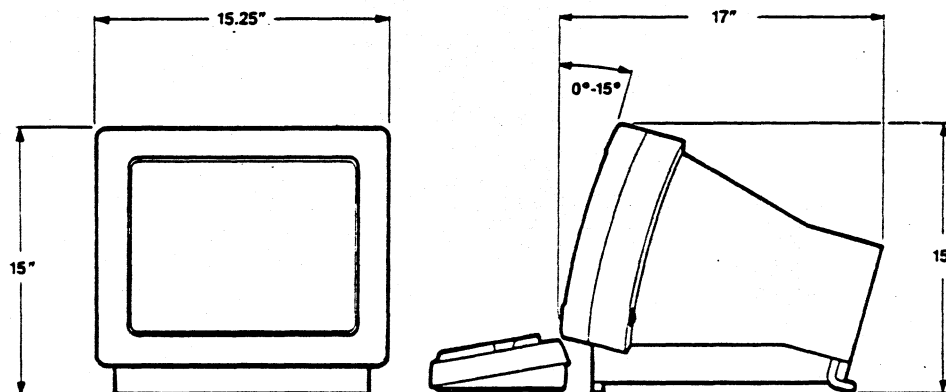
Interface/Mother board circuitry provides inter-connection of the logic, power supply, video and optional light pen circuitry.

Logic circuitry generates the timing signals for synchronization with other circuitry and processes data to generate video and communication signals.

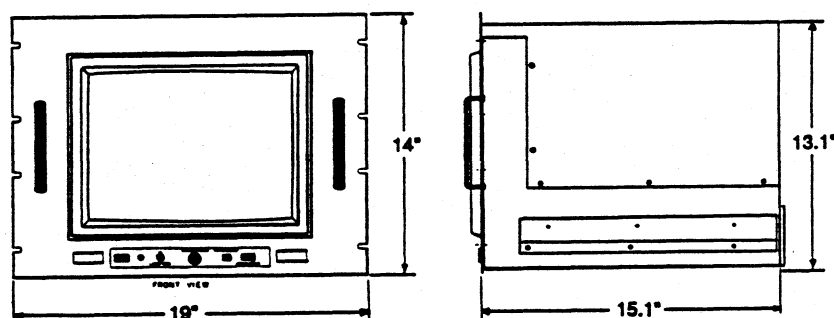
CRT displays characters and graphics generated by the Logic board.

3800 DESCRIPTION

Two units, similar to the 3810 and 3820 14" CRT terminals, incorporate the KM-3 or KM-4 Autoranging Power Supply, KM-3 or KM-4 Deflection, and TC-1 Video Amplifier assemblies. These terminals are called 3815 and 3825. All "Desk top" 3800 terminals use similar ergonomic plastic cabinets.



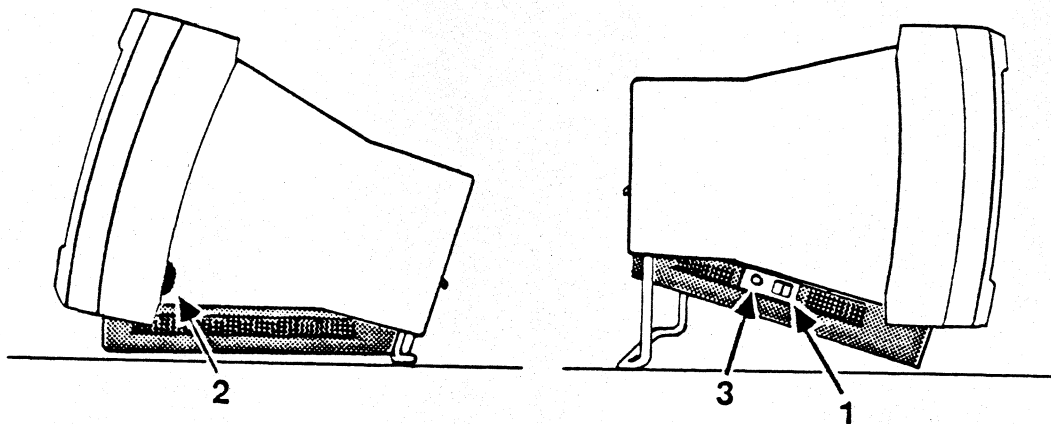
3865 and 3875 are rack-mount versions of 3815 and 3825 terminals which supersede the older 3860 and 3881 models. All rack-mount 3800 terminals use similar metal enclosures.



ALL 3800 units share the same wire frame chassis, and 14" CRT. 3800 units with the Dot Addressable Graphics board installed use #105119 Interface/Mother board. All other 3800 units use #103496 Interface/Mother board.

3800 CONTROLS

The 3815 and 3825 terminals share the same controls as the 3810. The 3865 shares the same controls as the 3860.



1. Power Switch. Turn the terminal on by pressing the side of the switch marked I. Turn the unit off by pressing the side of the switch marked 0.

2. Contrast Control. Use the contrast control to vary the difference between the display's light and dark elements. With a suitable image displayed on the screen, adjust the contrast control to achieve the best balance between image brightness and fine detail rendition. The optimum setting may vary with different types of displays and changes in ambient light level, as well as with individual taste.

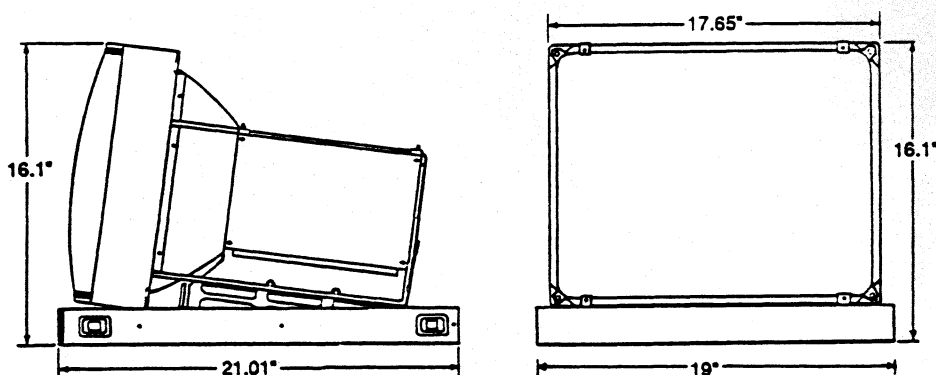
3. Manual Degaussing Button. The terminal is degaussed each time power is turned on. The manual degauss button may be used when additional degaussing is required during an operating session. Degaussing eliminates color impurities and other distortions in the display by neutralizing the effects of magnetic fields in the surrounding environment.

8800 DESCRIPTION

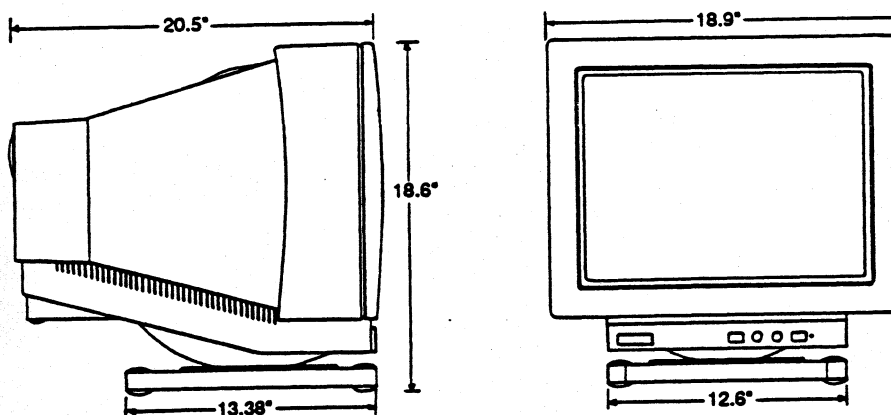
To improve 8800 Series 19" CRT terminals, the analog board used in 8810 and 8820 terminals was replaced by the AR-2 Auto-ranging Power Supply and the AR-2 Deflection modular printed circuit boards. Video signal amplification is provided by either a TC-3 Video Amplifier or an AR-2 Video Amplifier board.

The smaller modular circuit boards allow the use of a new wire frame chassis similar to the chassis in 3800 units. A two slot card cage and #105471 mother board are mounted to the bottom of the wire frame chassis for plug-in installation of the #105150 Logic and #105194 or #105408 Dot Addressable Graphics boards.

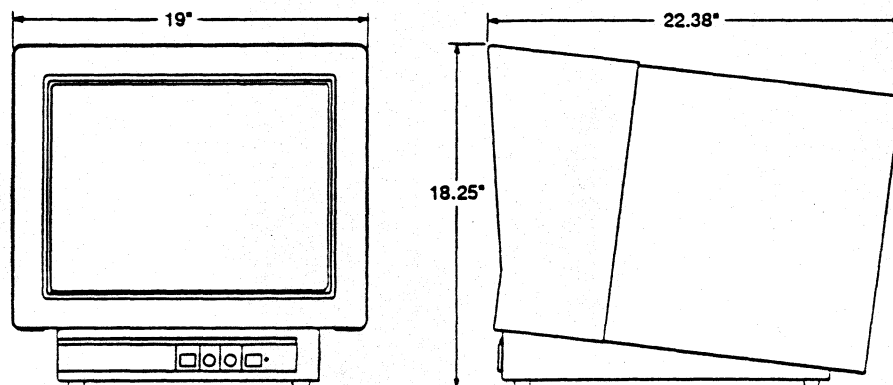
Two 8800 units are available with the new analog boards and the wire frame chassis mounted to the old style base pan foundation of the 8810. The 8814 and 8824 are console mount units shipped with no cover installed for OEM applications.



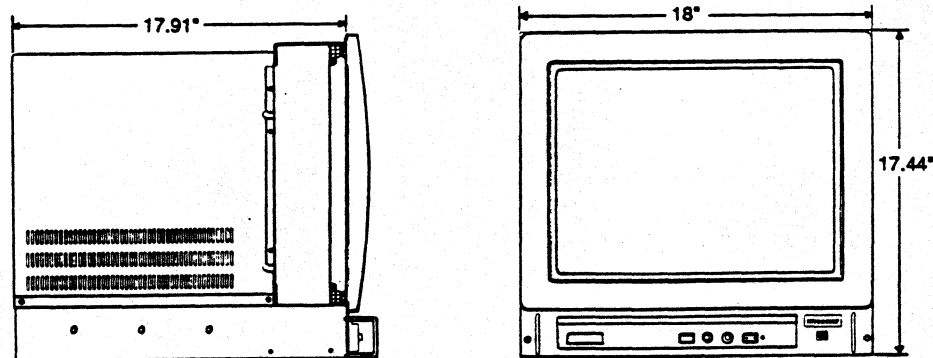
Two 8800 units feature a new plastic ergonomic cover with a tilt-swivel base and the new analog boards with the wire frame chassis. These terminals are called 8815 and 8825.



Two 8800 units designed to meet NEMA-2 standards are available. These units feature a desktop enclosure constructed of metal, which provides protection from falling dirt and liquids. The NEMA-2 terminals with the new modular analog circuitry and wire frame chassis are called 8816 and 8826.

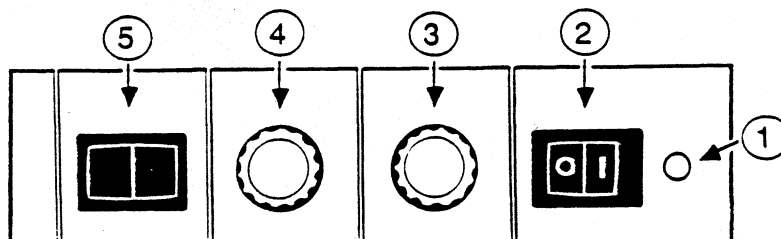


A 19" diagonal CRT rack-mount 8800 series terminal is available in two versions. Both 8800 rack mount units feature the analog boards and wire frame chassis of the 8815 and 8825. These new rack mount terminals are called 8865 and 8875.



8800 CONTROLS

The 8814, 8815, 8816, 8824, 8825, 8826, 8865, and 8875 controls are normally located in the front, below the CRT bezel. Some 8814, 8824, 8865, and 8875 terminals have the control panel installed in the rear of the unit. An additional receptical is provided with the controls to connect the keyboard from the front of the unit in the 8865 and 8875 Rack-mount 19" CRT terminals.



1. Status Indicator. The green LED on the right side of the power switch will be illuminated whenever the monitor is operating safely. The LED is not a power on indicator!!

IF THE LED IS NOT ILLUMINATED WITH POWER APPLIED AND TURNED ON, A FAULT HAS BEEN DETECTED BY THE UNIT AND ONLY THE HIGH VOLTAGE CIRCUITRY FOR THE CRT IS SHUT DOWN.

Circuit boards inside the unit still have power to them and standard safety precautions should be observed.

2. Power Switch. Turn the terminal on by pressing the side of the switch marked I. Turn the unit off by pressing the side of the switch marked 0.

3. Contrast Control. Use the contrast control to vary the difference between the display's light and dark elements. With a suitable image displayed on the screen, adjust the contrast control to achieve the best balance between image brightness and fine detail rendition. The optimum setting may vary with different types of displays and changes in ambient light level, as well as with individual taste.

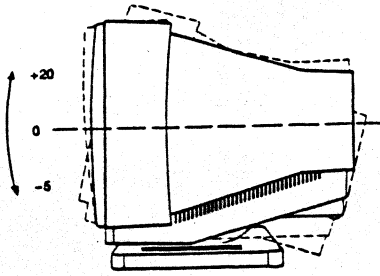
4. Brightness Control. Use the brightness control to adjust the overall intensity level of the display. After allowing the unit to warm up, adjust for the amount of brightness needed to make the display clearly visible.

5. Manual Degaussing Button. The terminal is degaussed each time power is turned on. Degaussing eliminates color impurities and other distortions in the display by neutralizing the effects of magnetic fields in the surrounding environment.

If the unit is left on continuously or is repositioned following power-up, the screen may pick up additional magnetic flux, causing the display colors to appear "blotchy" or otherwise distorted. If this happens, degauss the screen manually by pressing and releasing the degaussing button.

Manual degaussing may be repeated as required; but FOR FULL EFFECTIVENESS, ALLOW AT LEAST FIVE FULL MINUTES BETWEEN APPLICATIONS. Shorter intervals may result in incomplete removal of flux and residual color impurities.

If the unit is located near electric transformers, motors, loudspeakers, or other strong magnetic sources, degaussing alone may be insufficient. Try reorienting the unit relative to the magnetic source or increasing the distance between them.



6. Viewing Angle Adjustment. The tilt-swivel base of the 8815 and 8825 monitor cabinet allows a full 360-degree horizontal rotation. The display axis can be tilted vertically through a range of about 5-degrees below and above the horizontal.

ANALOG FEATURES

The analog circuitry featured in the units described in this Addendum provides improved performance and reliability of 3800/8800 Series terminals.

The Auto-ranging Power Supply

- * Intecolor developed a switching power supply that adjusts to line voltage and frequency variations automatically. Input line voltage may vary from 90 VAC to 250 VAC and line frequency may range from 40Hz to 70Hz. Output voltages are maintained even as line variations occur.
- * Fault detection circuitry in the Auto-ranging Power Supply will shut the unit off when input line voltage is below specifications, or if certain problems are detected by the circuitry.
- * Soft-start circuitry in the Auto-ranging Power Supply controls start-up of the switching circuitry to reduce stresses associated with extremely varied operating conditions.
- * Current limiting circuitry limits the maximum amount of current output from the power supply to a preset level to guard against short circuited boards.

Automatic Beam Current Limiting (ABL)

- * ABL circuitry (sometimes called Extended High Voltage Regulation or EHVR) limits the overall screen intensity to prolong the life of the CRT.
- * CRT average beam current is limited to a preset value to provide bright characters and detail while protecting the CRT from large areas of white background color.
- * Circuitry on the Video board and Deflection board work together to limit the gain of the video amplifier so that color quality does not depreciate when current limiting occurs.

3800/8800 LOGIC

Use of the terminal keyboard, diagnostic and logic functions is described in the existing INTECOLOR MAINTENANCE MANUAL for the 8800 & 3800 SERIES TERMINALS.

The 105150 Logic Board is installed in all 3800/8800 Series terminals and may feature either V1.70 or V2.00 firmware. To upgrade firmware in the field, see Appendix B of this Addendum.

Two Dot Addressable Medium Resolution Graphics Boards are available. The 105194 and 105408 are similar to the 102913 Dot Addressable Graphics Module used in earlier 3800/8800 Series units.

Circuitry of the 102913 Graphics Module was physically rearranged to make the 105194 Graphics Module, providing room for installation of a fan.

An optional 105408 Graphics Module is similar to the 105194 with larger capacity memory installed to include four pages of graphics screen memory. Software commands are available to access and display each of the four screens.

Circuit Description of the 105194 and 105408 Graphics Modules is similar to that of the 102913. See the Dot Addressable Graphics Module -- 8820 section in the existing maintenance manual. Schematic drawing #102911 is used for circuit analysis of 105194 and 105408 Graphics Modules.

The twelve screen memory IC's in the 105408 Graphics Module, UH6 through UH17 shown in the upper left quadrant of schematic #102911, are 64K X 4 dynamic ram 4464-type devices.

See Appendix D, for arrangement of the components on the PCB for 105194 and 105408 Graphics Modules.

Check the INTECOLOR MAINTENANCE MANUAL for the 8800 & 3800 SERIES TERMINALS for Functional Description of System, Software, Input/Output interface circuits, Applications, and Logic Board descriptions.

CHAPTER II

INSTALLATION

CHAPTER II

INSTALLATION

SPACE REQUIREMENTS

Space required by 3800 and 8800 series terminals may be judged with reference to the table of dimensions below. Additional clearance should be allowed at the rear and on either side of the monitor cabinet to allow access to connectors and controls. Some overhead clearance should also be allowed so that air can circulate freely about the unit.

Model	Height	Width	Depth
3815	15.00"	15.25"	17.00"
3825	15.00"	15.25"	17.00"
3865	14.00"	19.00"	15.50"
3875	14.00"	19.00"	15.50"
8814	16.10"	19.00"	21.01"
8815	18.60"	18.90"	20.50"
8816	18.25"	19.00"	22.40"
8824	16.10"	19.00"	21.01"
8825	18.60"	18.90"	20.50"
8826	18.25"	19.00"	22.40"
8865	17.40"	19.00"	17.90"
8875	17.40"	19.00"	17.90"

ENVIRONMENTAL CONSIDERATIONS

The relative humidity of the ambient air should be between 10% and 95% (non-condensing).

In especially dry environments, preventive measures against static discharge may be required to protect the terminals' internal components from damage.

The terminal should not be situated within **strong magnetic fields**, such as those present around power transformers and live voltage regulators. These fields can cause distortion and discoloration of the CRT display.

Dust and smoke particles can cause problems with most units because they are attracted by the units' high voltage components and can collect at ventilating holes as well as on the screen. The NEMA-2 enclosure provides protection against all but the finest dust particles.

ELECTRICAL REQUIREMENTS

The terminal is designed to draw power from **single-phase AC lines only**. Input voltage may vary from 90 VAC to 250 VAC.

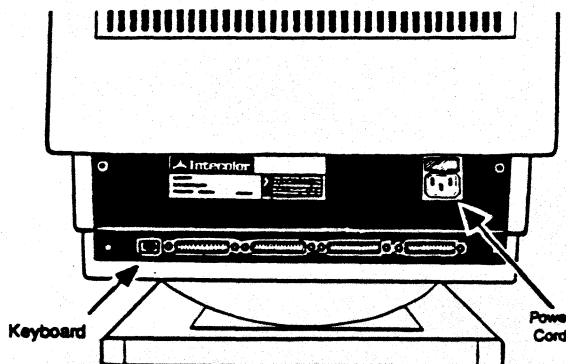
CAUTION: Under no circumstances should the unit be exposed to line voltages in excess of 250 VAC.

INTERCONNECTION

CAUTION: Be sure power switch is in the OFF position before connecting electrical power cord.

Power cord: Attach the power cord by plugging its female connector into the back of the terminal. Then plug the 3-pronged connector into a grounded outlet. If a three-pronged outlet is unavailable, provide an earth ground by using a 3-prong to 2-prong adapter whose green lead is grounded. Ground other units attached to the system and keep interconnecting cables as short as possible to minimize the risk of RF interference.

Keyboard: Connect the keyboard by plugging its RJ45S keyed telephone-type plug into the keyboard connector. Hold down the plug's lock-tab, slide it into the connector, and release the tab, making sure the plug is securely seated. To disconnect the keyboard, hold down the lock-tab and gently withdraw the plug.



Verify correct terminal operation before connecting it to a host or to any peripheral devices. See POWER ON section.

Host I/O: The panel on the back of the terminal provides four DB25 female connectors for host and peripheral connections in addition to the RJ45S keyboard connector.

Refer to the existing Intecolor Maintenance Manual for the 8800 & 3800 Series Terminals, page 3.06 for descriptions of all Host and I/O connections.

POWER ON

Switch the unit on by pressing the "I" edge of the power switch. The terminal performs diagnostic self-tests while the CRT warms up, then displays a header message in the upper left-hand corner of the screen, giving its model number and the firmware installed. For example:

INTECOLOR 8800 V2.0

WHEN THE TERMINAL DISPLAYS ITS HEADER, IT IS READY FOR USE.

The number following "V" is the currently installed firmware version.

If no message is displayed, or an error code appears on screen, the power-on diagnostics have not been completed satisfactorily. The terminal will not operate properly until it completes these tests, so turn off the power and turn it back on after a brief pause. Usually this solves the problem, since many difficulties are due to brief power-line irregularities. If an error code is still displayed, it identifies the area where a problem has been found.

Code	Meaning
ROM	Check Read-Only Memory
NONV	Check Non-volatile Memory used for Set-up Parameters
SCRN	Check Screen Memory
HOST	Host I/O Problem
KEYB	Keyboard/Printer Problem

CHAPTER III

DIAGNOSTIC TESTS

CHAPTER III

DIAGNOSTIC TESTS

SETUP MENU

The most fundamental checkout is performed by accessing the terminal's Setup menus. These menus let you display the terminal's configuration, set essential parameters, and perform some basic tests. To access the Setup menus, hold down the Shift key and press the Setup key. This causes the main Setup Menu (the Host I/O Menu) to be displayed and, through it, lets you access the other Setup menus and displays. The main Setup Menu looks something like this:

	Local/Line	On line
	Echo	Off
	Flow Control	^S^Q
H	Backspace Code	^H
O	Protect	Disable
S	Data Rate	9600
T	Stop Bits	1 Stop Bit
	Parity	8 bits, none
I	OTHER MENU	OPERATOR PREFERENCE
/		CONFIGURATION REPORT
O		
	Special Selections	
M	1. SAVE current setup menu.	
E	2. RECALL old setup menu.	
N	3. Recall FACTORY Default Setup Menu.	
U	4. Recall '8001G' Default Setup Menu.	
	5. Exit through Self Tests.	

Arrow keys	select an item
Return	ends Setup Mode

Whenever you want to return to this main Setup menu, you must enter the Shift-Setup combination.

This menu lets you set fundamental parameters for host communications. The factory default values are shown in the right-hand column above. Use the cursor control (arrow) keys to select an item for change. The HOME key may be used as a toggle input to make the change.

To exit Setup, press the Return key.

AUTOMATIC SELF-TESTS

The Automatic Self-Test routines are entered at power-up. They run one time without interruption, unless an error is detected. These same automatic self-tests may also be run in a continuous "loop".

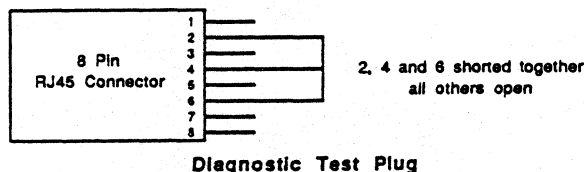
Continuous Self-Tests may be initiated from the keyboard or by using a Diagnostic Test Plug. Once started, they will run until

- an error is detected, or
- an outside condition causes interruption

Use the **keyboard** (locally) to enter SETUP and access the Host I/O Menu. Push "5" to begin the diagnostic self-tests. When initiated in this manner, the self-tests run indefinitely until an error is detected. Press the Setup key to stop the tests.

In applications where the terminal is not fitted with an Intecolor Keyboard or where a special function keyboard is used in place of the standard Intecolor Keyboard, a **Diagnostic Test Plug** may be used to initiate Continuous Self-Tests.

A Diagnostic Test Plug can be fabricated by shorting together pins 2, 4, & 6 on an 8-pin RJ45 Male Connector.



Diagnostic Test Plug

To start the continuous self tests with the test plug:

1. Turn power off.
2. Unplug the keyboard connector and plug the test plug into the keyboard port.
3. Turn power on.

When initiated in this manner, the self-tests run indefinitely until an error is detected or the unit is shut down.

Do not allow the continuous diagnostic tests to proceed unattended. These are primarily intended for confidence testing and as a troubleshooting aid. Since they do not include automatic retry, they cannot distinguish true hardware failures from the apparent failures caused by line surges, noise, and the like. Hence, their use in a continuous loop for burn-in testing will give misleading results. Errors reported must always be verified and only after an error has been reported consistently in each of several test runs. Each test run should be initiated by cycling the power. A reported condition may only be verified in this manner.

In relation to this statement, take note of the following:

1. Continuous tests may be interrupted by a momentary power failure. This will result in one of the following:
 - * Reset of the terminal and display of the header message.
 - * Display of the Host I/O Menu (only in some cases.)
 - * Screen goes blank, if the unit was operating with the CRT Saver feature on. Entry of any character from the keyboard will bring back the display.
2. Power glitches or other strong electrical interference may result in a minor data error. This will cause an error display or suspension of a test.
3. If the Continuous Self-Test routine stops, or if an error indication appears, the test should be restarted. If a problem actually exists, the unit will fail a second time with the same indications.
4. If an error still exists on the second and third time around, the type of screen display and the logic board LED pattern should be noted.

Refer to the existing Intecolor Maintenance Manual for the 8800 & 3800 Series Terminals, appendix G for a description of Logic Diagnostic LEDs.

PORT TESTS

Another series, called Port Tests, may only be initiated from the Host I/O Menu, accessible through SETUP.

From the Host I/O Menu (SETUP), a Submenu of PORT TESTS (below) may be displayed on screen by pushing the "6" on the keyboard.

SELF TESTS MENU

1. Host and Aux port tests
2. Parallel port test
3. Printer port test
4. Quit: Reset system

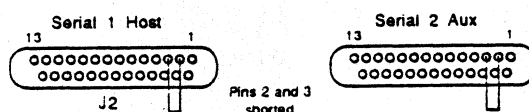
Enter your choice

Each test begins when a key is pressed. Results of the tests are reported on the screen, concluding with a pass or fail indication. When a key is pressed again, the Port Tests Submenu returns.

In order to use these tests, **JUMPER** connections must be installed as described below. When one of the tests is chosen, a reminder to use the jumper(s) is included in the display.

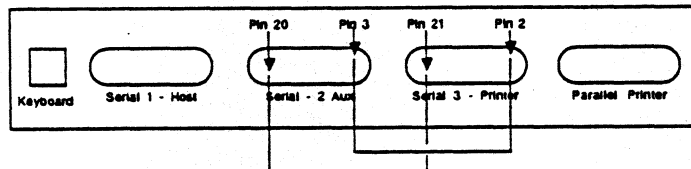
- "1" Testing either the Serial 1-Host or the Serial 2-Aux Ports require a jumper between pins 2 and 3 of each port.

Host and Aux Test



- "3" Testing the Printer Port requires that a cable be connected from Serial 3-Printer port pin 2, to Serial 2-Aux port pin 3; and another cable between Serial 3-Printer port pin 21 to Serial 2-Aux port pin 20.

Printer Port Test



Selection of a Port Test from the submenu will result in the following displays:

```

| Host & Aux Test
|   "1"   Insert Host and Aux jumpers
| Hit any key
| ~~~~~
  
```

(Since the parallel port option is not supported in the standard terminal, use of the "2" key brings up a display with instruction to abort.)

```

| Serial Printer Test
|   "3"   Insert Printer/Aux jumper
| Hit any key
| ~~~~~
  
```

- "4" Results in exit from Setup via one cycle of the Automatic Self Test Routine, followed by reset.

SERIAL I/O PORT TEST

Operation of the Serial 1-HOST port may be verified by entering data from the keyboard when the terminal's Setup parameters are set to "ON LINE" communications, with ECHO "OFF".

To perform this test, terminals 2 and 3 of the Serial 1-Host port (J2) must be connected by a shorting plug.

1. Push Shift + Setup simultaneously to bring up SETUP.
2. Use an Arrow Key to to change the mode of operation back to the factory default value "ON LINE". Then, push RETURN.
3. After installing the jumper, described above, the display screen will reflect any data that is entered at the keyboard. Keyboard inputs will go to the serial output port (pin 2 of J2) and will return via the jumper to the serial input port (pin 3 of J2) for display on the screen. With the jumper plug removed, operation of the keyboard will not result in display.
4. Return to Setup to select and save the desired parameters for further use of the terminal.

ANALOG DIAGNOSTIC CHECK

This procedure describes a quick diagnostic check to determine the performance of the analog boards used in 3800/8800 Series terminals. The covers of the unit need not be removed to perform these checks.

COMPLETE ALL STEPS WHEN POSSIBLE BEFORE PROCEEDING TO THE ALIGNMENT PROCEDURES OR TROUBLESHOOTING CHARTS.

1. Turn the power on and wait 60 seconds for the unit to warm up. The model number and version of firmware should be displayed in green, yellow, magenta, and cyan single height characters in the upper left corner of the screen.
2. Hold down the "SHIFT" key and press the "SET UP" key, then release both keys. Verify that "LOCAL" is high-lighted. If not, press and release the "HOME" key to toggle between "LINE" and "LOCAL".
3. Press and release the "FG ON", "white dot", "ESC", "Y", and "E" keys. Observe a full screen of single height E's.

4. Check the characters for solid white letters, vertical linearity, horizontal linearity, position stability, distortions, and video noise.

The screen of the CRT can be flooded with selected solid colors by pressing and releasing the "BG ON", the key with the desired color dot, and the "ERASE PAGE" key.

5. One at a time display a full red, blue, and green screen.

Check each display for video noise and that it is centered both horizontally and vertically.

If 19" CRT, check each display for 13" width by 9 3/4" height.

If 14" CRT, check each display for 9 1/2" width by 7 1/8" height.

Automatic Beam Current Limiting (ABL)

Perform the following checks on all units equipped with ABL circuitry. 3810, 3820, 3860, 8810, and 8820 terminals are not equipped with ABL circuitry.

6. Display a black screen.
7. Flood the display with a full white screen. The screen intensity should decrease within one second after initial white screen is displayed.

If the display fails any of the **Analog Preventive Maintenance checks** perform the alignment procedures outlined in Chapter IV or see the troubleshooting charts in Chapter V.

CHAPTER IV

ALIGNMENT PROCEDURES

CHAPTER IV

ALIGNMENT
PROCEDURES

INTRODUCTION

All Intecolor terminals are completely adjusted and thoroughly tested before shipment from the factory. 3800 and 8800 terminals are shipped with preconverged in-line cathode ray tubes installed. Convergence adjustments associated with delta gun CRTs are not required.

A complete alignment in the prescribed order should be performed when repairs are completed, or the display fails the Analog Diagnostic Check (pg. III.5)

Two alignment procedures are provided:

Section One 3800 describes the alignment of 3815, 3825, 3865 and 3875 terminals. This section begins on page IV.3.

Section Two 8800 describes the alignment of 8814, 8815, 8816, 8824, 8825, 8826, 8865 and 8875 terminals. This section begins on page IV.13.

Perform all of the adjustment procedures in the order presented by this manual. Any adjustments performed out of sequence must be followed by a complete check of all alignments in the prescribed order.

Read the entire procedure and determine the location of adjustable components before beginning alignment.

The cover must be removed to perform the adjustments described. See Appendix C for instructions of cover removal.

WARNING! Any maintenance performed with power on and covers off subjects the operator to electrical shock that could cause injury or death. Only properly trained and qualified technicians who are aware of the existing hazards should attempt this level of maintenance.

WARNING! Operate the unit on single phase AC power only. The power supply protection circuit is designed for single phase only. The upper line voltage limit of 250 VAC must not be exceeded; the line filter, fuse, fuseholder, and switch are rated at 250 VAC maximum.

WARNING! For the technician's safety, it is recommended that an isolating transformer be used between the unit and the AC voltage supply.

Tools and Equipment Required

1. Shaft insulated, flat blade screwdriver (1/8" tip)
2. 3/32" hex, plastic alignment tool
3. Multimeter, Fluke 8020B or similar
4. High Voltage Probe, 40KV rating
5. Oscilloscope, DC to 15 MHz.
6. 0-1 DC Milliammeter, insulated for at least 35KV, with connectors for insertion into the CRT path.
7. Isolation transformer for line AC.

Warm-up

Allow the terminal a full 20 minutes to warm-up before proceeding with the alignment. After this initial warm-up, the terminal may be shut down for short periods so that test equipment may be connected or disconnected. In all cases, the temperature should be fairly stable when final adjustments are made.

Preliminary Adjustments

Press the degauss button during the warm-up period to ensure that the terminal is fully degaussed. Turn the contrast control (and brightness control on 8800 Series terminals) to the full clockwise position.

Line Fuse

The line fuse installed in 3800 and 8800 units with the auto-ranging power supply should be a 5mm X 20mm, 4.0A, 250V Slow Blow type fuse.

Line Voltage and Frequency

The auto-ranging power supply adjusts automatically to line voltage variations in the range of 97 to 250 VAC and line frequency variations from 40 to 70 Hz. The auto-ranging power supply provides stable output voltages even as changes in line voltage and frequency occur.

Assembly Number

More than one version of some assemblies may be used in a series of terminals. For example; either of two different video assembly boards may be installed in 8814, 8815, 8816, 8824, 8825, 8826, 8865 and 8875 terminals. The part number for each modular assembly is printed on a sticker which normally can be found on the component side of the PCB.

SECTION ONE 3800

The following alignment procedure is intended for maintenance and alignment of 3815, 3825, 3865, and 3875 terminals. While not specifically intended for troubleshooting, they may also serve as diagnostic tools.

The instructions are given in step-by-step form and in the recommended order of execution. Direction of rotation is specified when adjusting from the back of the printed circuit board.

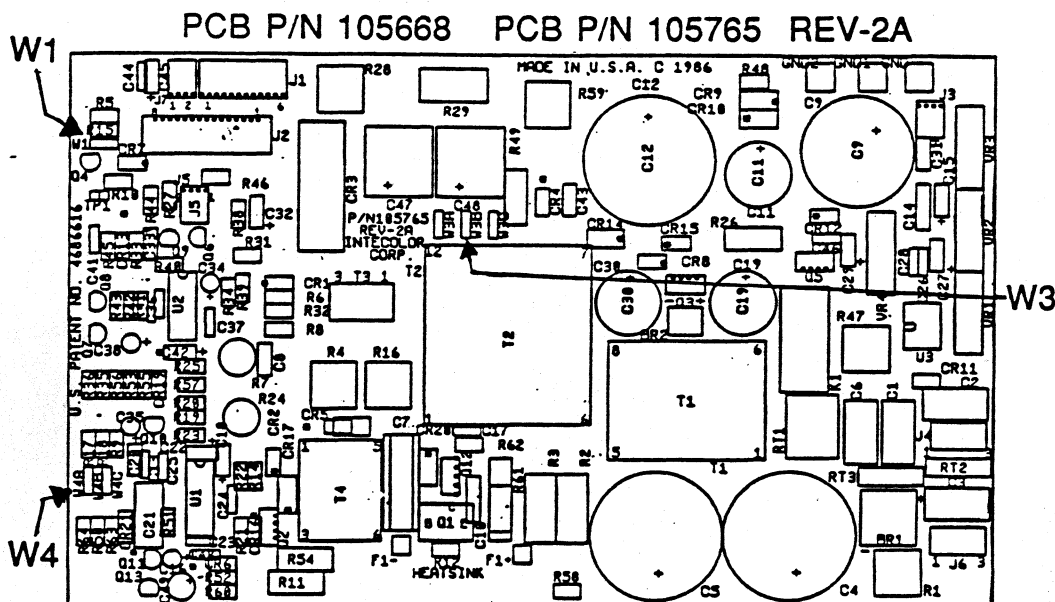
PRELIMINARY

Before beginning alignment, technicians should verify that all jumpers are in the correct position and become familiar with the location of adjustable components. The adjustable components should be set at the suggested pre-set positions if a board has been repaired or replaced, or the technician suspects gross mis-adjustment.

Power Supply Jumpers

The following table lists the proper jumper configuration for both the #105669 KM-3 and the #105766 KM-4 power supply when used in 3800 Series terminals.

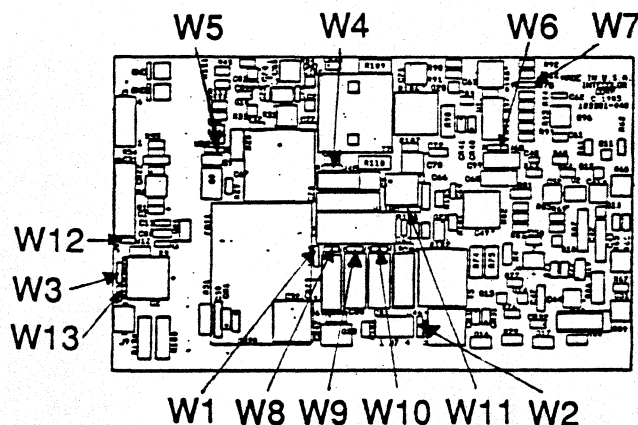
KM-3 and KM-4		Function
W1	on	disconnects HSYNC from PS
W2	hard wired	not used
W3	A	selects V1 output voltage
W4	A	selects PS switching frequency



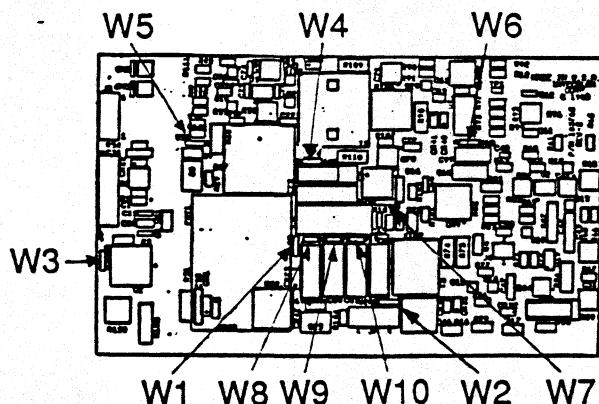
Deflection Jumpers

The following table lists the proper jumper configuration for the #103302 KM-3 and #105763 KM-4 deflection boards when used in 3800 Series terminals.

KM-3	KM-4	Function
W1 B	W1 B	selects source for G1 voltage
W2 off	W2 B	selects cathode bias voltage
W3 A	W3 A	selects filament voltage
W4 A	W4 A	selects capacitor for Hor. width ckt.
W5 A	W5 A	selects feedback for HV adjust
W6 A	W6 A	selects frequency of Hor. oscillator
W7 A		selects Hor. oscillator feedback
	W7 A	selects inductor for Hor. width ckt.
W8 off	W8 off	selects filter capacitor for V2
W9 on	W9 on	selects filter capacitor for V2
W10 off	W10 off	selects filter capacitor for V2
W11 A		selects inductor for Hor. width ckt.
W12 on		alternate selection of G1 voltage
W13 on		bypasses the optional brightness pot.



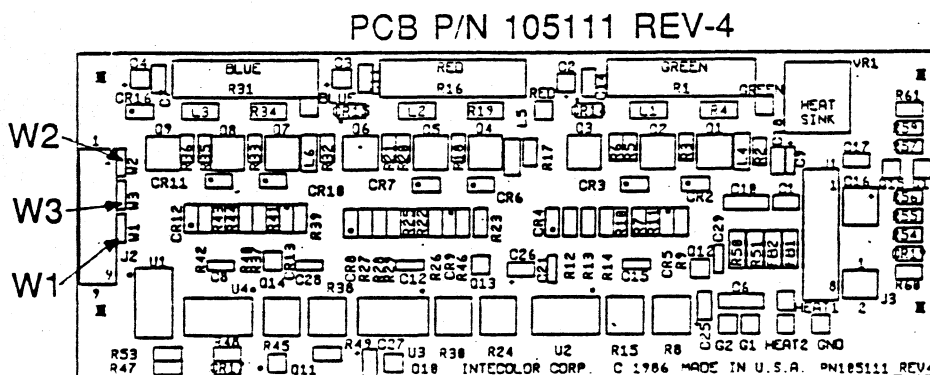
PCB P/N 103301
KM3 DEFLECTION REV-4



PCB P/N 105762 REV-2
KM4 DEFLECTION

Video Jumpers

The #105112 TC-1 video board was designed to process one or two bit logic. Jumpers W1, W2, and W3, should be installed for one bit operation as is the output from Intecolor 3800 series terminals.

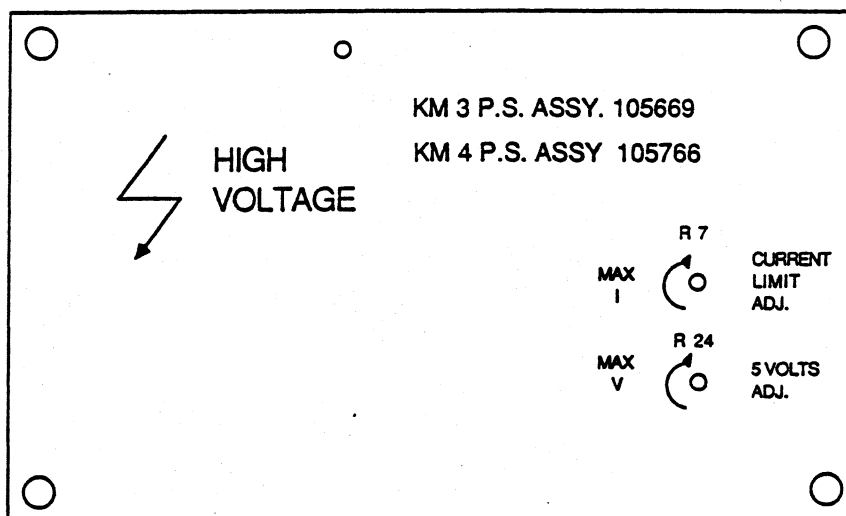


TC-1 Video

Power Supply adjustable components

The following list describes the adjustable components for both the #105669 KM-3 and #105766 KM-4 power supplies when used in 3800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
* R24	+5 VDC output adjust	Mid-range
* R7	Current limit adjust (Pre-adjusted at the factory using special loads)	DO NOT ADJUST!

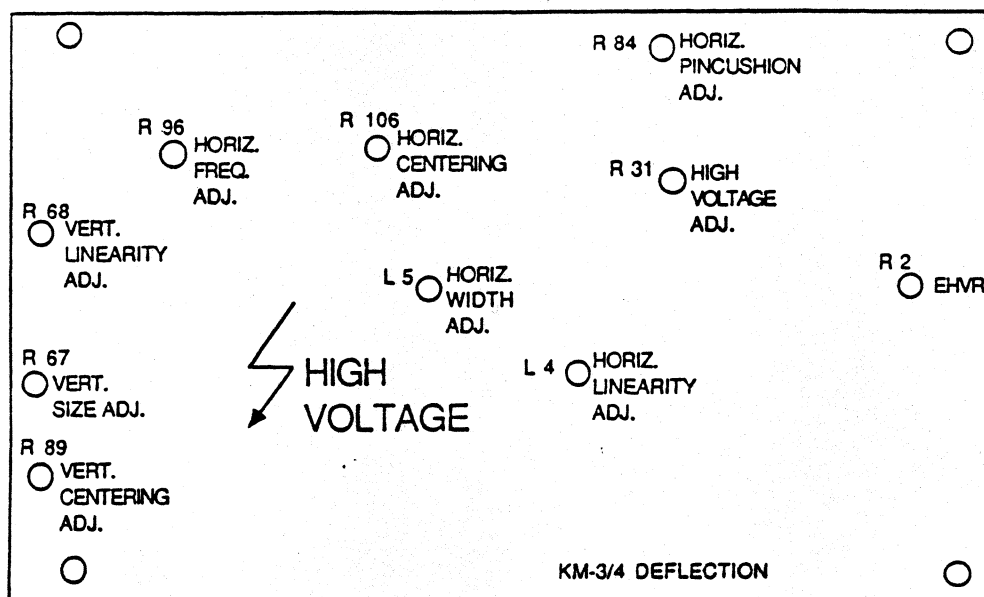


KM-3 and KM-4 Power Supply

Deflection Adjustable Components

The following list describes the adjustable components for both the #103302 KM-3 and #105763 KM-4 deflection boards when used in 3800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
R68	Vertical linearity	Mid-range
R67	Vertical height	Mid-range
R89	Vertical centering	Mid-range
R84	Horizontal pincushion	Mid-range
R96	Horizontal frequency	Mid-range
R31	High voltage	Full CCW
L4	Horizontal linearity	Mid-range
L5	Horizontal size	Mid-range
R106	Horizontal centering	Mid-range
R2	ABL	Mid-range

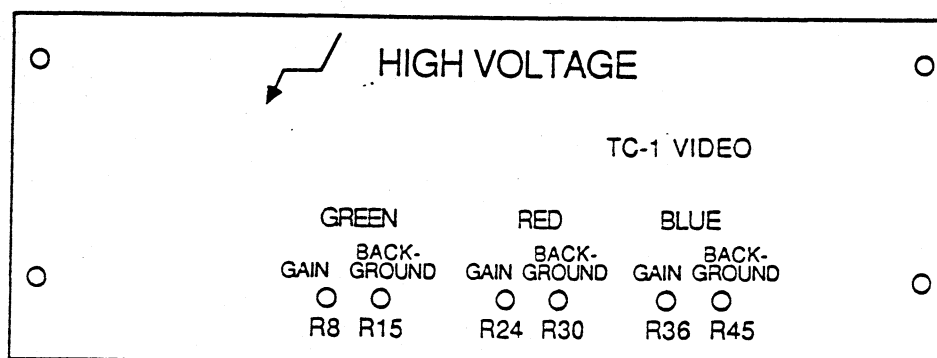


KM-3 and KM-4 Deflection

Video Adjustable Components

The following list describes the adjustable components for the #105112 TC-1 video board when used in 3800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
R8	Green Gain	Mid-range
R15	Green Background	Full CCW
R24	Red Gain	Mid-range
R30	Red Background	Full CCW
R36	Blue Gain	Mid-range
R45	Blue Background	Full CCW



TC-1 VIDEO

3800 ALIGNMENT PROCEDURE:**STEP ONE**

The adjustable components described in this step are located on the power supply module.

+5 VDC Adjust and Output Voltages

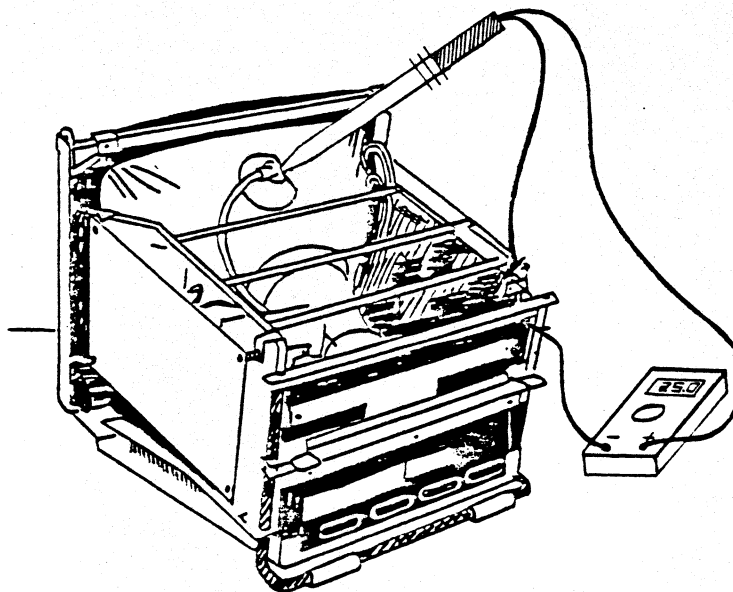
1. **Power Off.** Connect voltmeter to the +5 VDC test point on the logic board and a logic board ground test point. Apply power to the unit and wait 60 seconds.
2. Check voltmeter for reading of +5.1 VDC (+/- .1 V). Adjust for this voltage with potentiometer R24.
3. Check J2, pin 4 for +12 VDC (+/- .6 V).
4. Check J2, pin 6 for -12 VDC (+/- 1.2 V).
5. Check J2, pin 1 for +16 to 20 VDC.
6. Check J2, pin 3 for V1 (+85 to +95 VDC).
- 7. **Power Off.**

STEP TWO

The adjustable components described in this step are located on the deflection module.

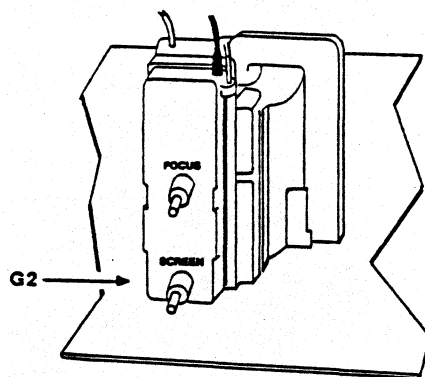
High Voltage

1. With the **Power Off.** Slip the high voltage probe tip under the anode cap of the CRT. Metal to metal contact must be maintained at the probe tip and the metal anode clip. Connect the ground lead of the high voltage probe to the metal wire frame chassis for a secure ground. (See the drawing on page IV.8).



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

2. Turn the unit on and wait 60 seconds for it to warm up.
3. Adjust R31 for a preliminary HV of 25KVDC.



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

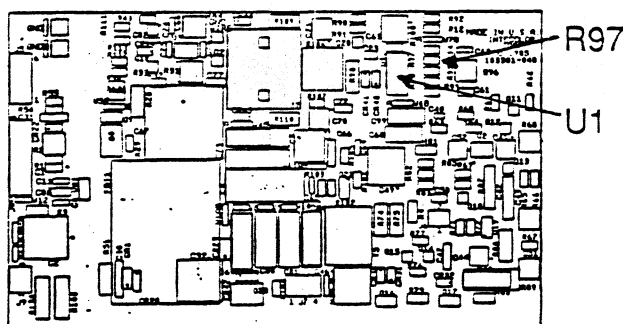
4. Adjust G2 (on flyback transformer) clockwise until raster scan lines are visible then rotate counter-clockwise until no raster is visible.
5. Adjust R96 if the video is unstable.

Verify that the terminal is in the Local mode by holding down the shift key and pressing the setup key. "Local" should be high-lighted. If it isn't, press the Home key to toggle from "Line" to "Local".

6. Get a blank screen by pressing and releasing the "BG", "black dot" and "ERASE PAGE" keys.
7. Adjust R31 for 25KVDC (+/- 200 VDC). If a raster scan becomes visible on the screen, turn G2 (on the flyback transformer) counter-clockwise until the raster just disappears.
5. Power Off. Disconnect the HV probe.

Horizontal Deflection Oscillator

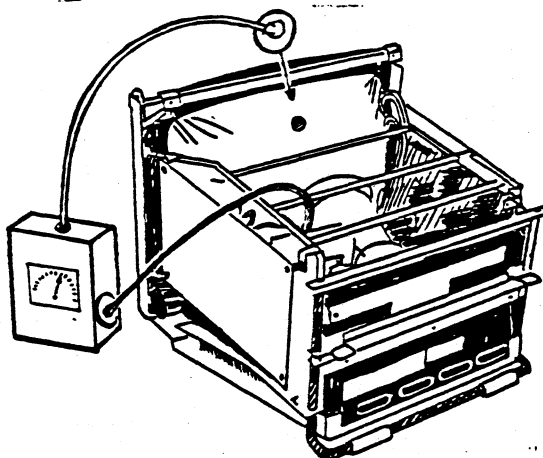
1. With Power Off, connect the voltmeter to R97 (leg farthest from U1) and ground.



2. Apply power to the unit and wait 60 seconds.
3. Adjust R96 for +6.0 VDC on the voltmeter. Turn power off and disconnect the voltmeter.

Automatic Beam Current Limiting

1. With Power Off, connect insulated milliammeter in series between the anode cap and the CRT.



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

2. Turn the unit on and wait 60 seconds.
3. Flood the screen with white by pressing and releasing the "BG" key, "white dot" key, and "ERASE PAGE" key.
4. Adjust R2 for 400 micro-amps on the milliammeter.

NOTE: If CRT beam current is too low the Video board may need adjustment first. Rotate R2 clockwise $3/4$ turn and proceed to STEP THREE. Return to this adjustment after completing the adjustments described in STEP THREE.

STEP THREE

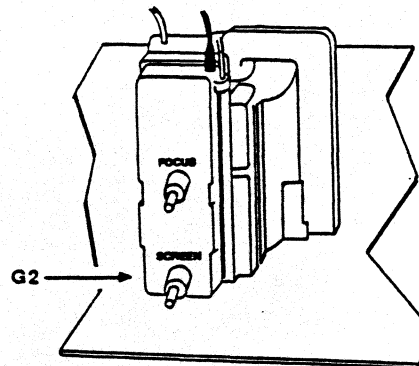
The adjustable components described in this step can be found on the video amplifier module.

NOTE: It is very important that the terminal be on for the full 20 minute warm-up period before starting the alignment of the video circuitry.

Background adjustment

1. Get a blank screen by pressing and releasing the "BG ON", "black dot" and "ERASE PAGE" keys.

Rotate the G2 control, on the deflection flyback transformer, clockwise until raster scan lines are visible. Then rotate the G2 control counter-clockwise until the raster just disappears.



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

2. With R15, R30 and R45 in the full CCW position, rotate the G2 control clockwise until the raster is just visible. Decide which color is predominant in the raster: red, green, or blue.

3. Leave the background potentiometer of the predominant color in the full counter-clockwise position. Adjust either or both of the two remaining background potentiometers clockwise for a gray raster on the screen.
4. Turn the G2 control counter-clockwise until raster scan lines disappear.

Gain adjust

The screen of the CRT can be flooded with selected solid colors by pressing and releasing the "BG ON" key, the key with the desired color dot, and the "ERASE PAGE" key.

1. Flood the screen with red. Adjust R24 for 168-178 micro-amps on the milliammeter.
2. Display a full green screen. Adjust R8 for 220-230 micro-amps on the milliammeter.
3. Now display a full blue screen. Adjust R36 for 168-178 micro-amps on the milliammeter.
6. Flood the screen with white. Check the display for uniform white color across the screen.

NOTE: If the CRT beam current is not limited to 400 micro-amps, perform the Automatic Beam Current Limiting adjustments described in STEP TWO.

STEP FOUR

The components described in this step can be found on the deflection module.

Display Size, Centering, and Focus

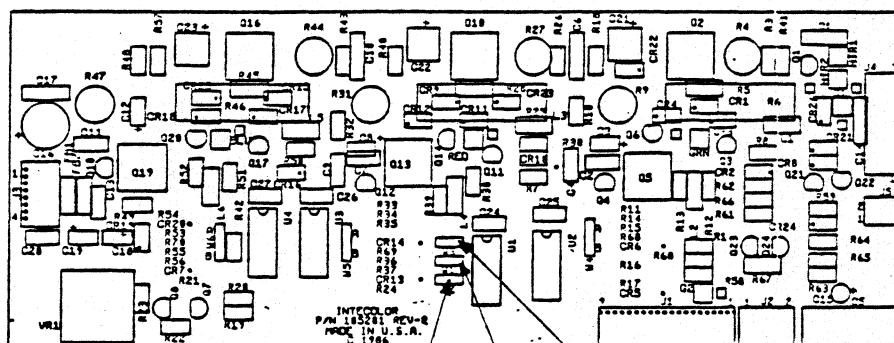
1. Get a blank display on the screen. Flood the screen with white E's by pressing and releasing the "FG ON", "white dot", "ESC", "Y" and "E" keys.
2. Adjust focus control for crisp, clear characters. (See the drawing of the flyback transformer on page IV.10).
3. Check the letters for uniform vertical size. Adjust R68 for vertical linearity.
4. Check the letters for uniform width. Adjust L4 for horizontal linearity.
5. Flood the display with any color.
6. Check the display for 7 1/8" (181mm +/- 3mm) vertical height. Adjust R67 as required.

7. Check that the display is centered vertically. Adjust R89 to move the display up or down.
8. Check horizontal width of display for 9 1/2" (241mm). Adjust L5 to change the width of the display.
9. Check that the sides of the display are straight. Adjust R84 if the sides are not straight.
10. Check the horizontal centering of the display. Adjust R106 to move the display from side-to side.
11. Verify the adjustments performed in this STEP. Screen size and character linearity are subject to change slightly, due to interaction of the circuitry.

Video Jumpers

The three jumpers W1, W2, and W3, should be installed on the TC-3 Video.

PCB P/N 105201
REV-2

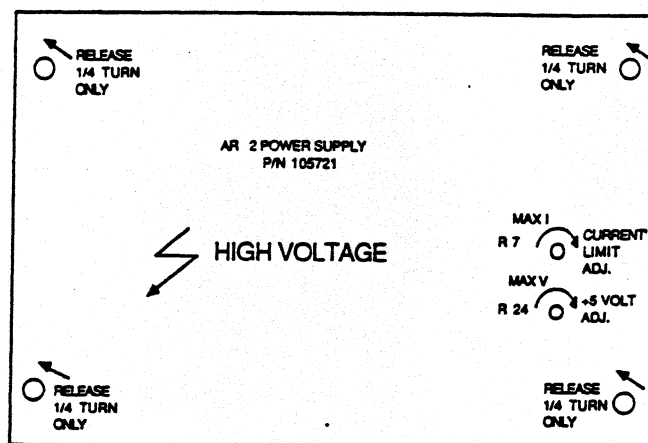


TC-3 Video W2 W1 W3

Power Supply Adjustable Components

The following list describes the adjustable components for the #105684 AR-2 power supply when used in 8800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
* R24	+5 VDC output adjust	Mid-range
* R7	Current limit adjust (Pre-adjusted at the factory using special loads)	DO NOT ADJUST!

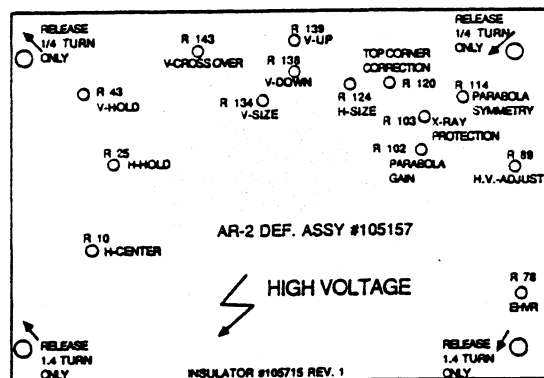


AR-2 Power Supply

Deflection

The following list describes the adjustable components for the #105157 AR-2 deflection board when used in 8800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
R10	Horizontal centering	Mid-range
R43	Vertical hold	Mid-range
R25	Horizontal hold	Mid-range
R78	ABL	Mid-range
R89	High Voltage	Do Not Adjust
R102	Parabola gain	Mid-range
R103	X-Ray protection	Full CCW
R114	Parabola symmetry	Mid-range
R120	Top corner correct	Full CCW
R124	Horizontal size	Mid-range
R138	Vertical down	Full CCW
R139	Vertical up	Full CCW
R134	Vertical size	Mid-range
R143	Vertical crossover	Full CCW

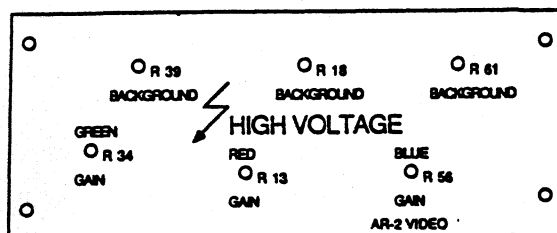


AR-2 Deflection

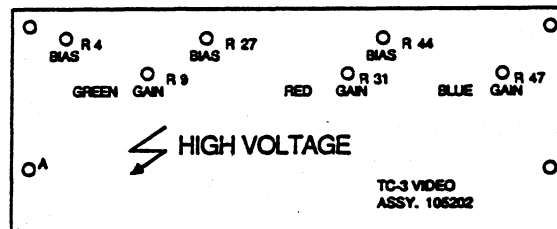
Video

The following list describes the adjustable components for the #105202 TC-3 video and the #105199 AR-2 video amplifier boards when used in 8800 Series terminals. Pre-set adjustments are provided but may not always be necessary.

Component	Function	Pre-set
TC-3 AR-2		
R9 R34	Green Gain	Mid-range
R4 R39	Green Background	Full CCW
R31 R13	Red Gain	Mid-range
R27 R18	Red Background	Full CCW
R47 R56	Blue Gain	Mid-range
R44 R61	Blue Background	Full CCW



TC-3 Video



AR-2 Video

8800 ALIGNMENT PROCEDURE:

STEP ONE

The adjustable components described in this step can be found on the power supply module.

+5 VDC Adjust and Output Voltages

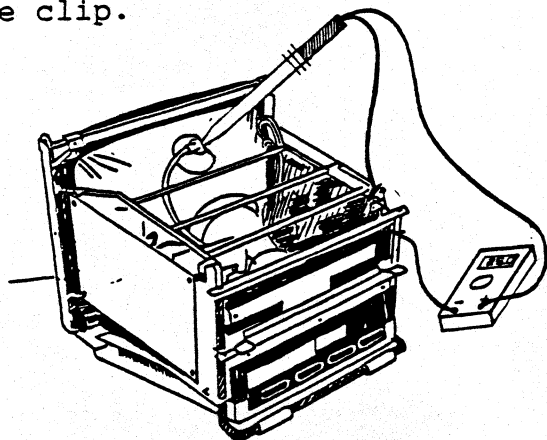
1. **Power Off.** Connect voltmeter to the +5 VDC test point on the logic board and a logic ground test point. Apply power to the unit and wait 60 seconds.
2. Check the voltmeter for reading of +5.1 VDC (+/- .1 V). Potentiometer R24 may be used to adjust the +5 VDC.
3. Check J1, pin 1 for -16 VDC (+/- 1.4 V)
4. Check J1, pin 3 for +16 VDC (+/- 1.4 V)
5. Check J1, pin 5 for +28 VDC (+/- 1.6 V)
6. Check J1, pin 7 for +90 VDC (82 to 92)
7. Check J2, pin 4 for +12 VDC (+/- .6 V)
8. Check J2, pin 6 for -12 VDC (+/- .6 V)
9. Check J8, pin 3 for +12 VDC (+/- .6 V))

STEP TWO

The adjustable components described in this step can be found on the deflection module.

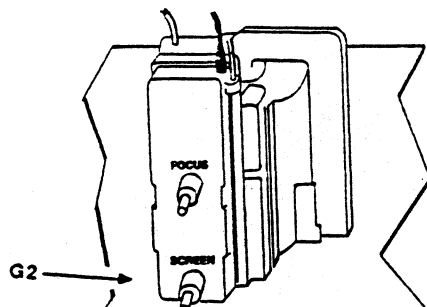
High Voltage and X-Ray protect

1. **Power Off.** Connect the ground lead of the high voltage probe to the wire frame chassis. Securely slip the high voltage probe tip under the anode cap of the CRT. Metal to metal contact must be maintained at the probe tip and the metal anode clip.



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

2. Apply power to the unit, wait 60 seconds.
3. Adjust R89 for preliminary HV setting of 25KVDC.
4. Adjust G2 (on flyback transformer) clockwise until rasters appear and then adjust counter-clockwise for no rasters.



WARNING! Extreme high voltage potentials exist in the flyback transformer.

5. Adjust R25 if the display is not stable
6. Adjust R43 if the video rolls vertically.
7. Slowly adjust R89 clockwise and observe that the HV drops off between 28 and 29KVDC. If a raster scan becomes visible on the screen, turn G2 (on the flyback transformer) counter-clockwise until the raster disappears.

Once the X-ray protect circuitry is activated, **turn the unit off to reset the circuitry** and turn R89 CCW 1/4 turn.

Perform the following Xray adjust procedure **ONLY IF THE UNIT DOES NOT SHUT DOWN AT THE PROPER VOLTAGE.**

X-Ray adjust

- A. **Power Off.** Adjust R89 and R103 fully counter-clockwise.
- B. Turn the power on and wait 60 seconds. Adjust R89 clockwise until the voltmeter reads 29KV.
- C. While observing the voltmeter, slowly adjust R103 clockwise until the HV output drops out.
- D. **Power Off.** Turn R89 fully counter-clockwise.
- E. Turn the power on and wait for the unit to stabilize. Slowly adjust R89 counter-clockwise while observing voltmeter. HV output should drop out between 28KV and 29KV.
- F. **Power Off** (to reset the X-ray circuitry).

- 8 Turn the **Power on**, and wait 60 seconds.

Verify that the unit is in local mode by holding down the Shift key and pressing the Setup key and observing that "LOCAL" is high-lighted. If "LOCAL" is not high-lighted, press the "HOME" key to toggle from "LINE" to "LOCAL".

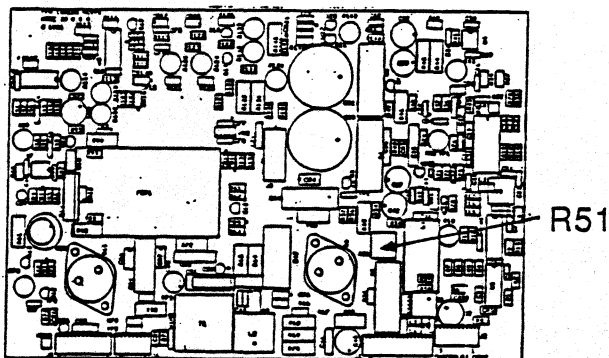
8. Get a blank display on the screen by pressing and releasing the "BG ON", "black dot", and "ERASE PAGE" keys.
9. Adjust R89 for 25KV (+/- 200 VDC) on the voltmeter.
5. **Power Off** and disconnect the HV probe.

Horizontal and Vertical Hold

1. **Power Off.** Disconnect connector plug P2 from J2 of the deflection board.
2. Apply power to the unit and wait 60 seconds. The video will roll across the screen from side to side.
3. Adjust R25 until the video on the screen almost stops rolling.
4. **Power Off.** Connect P2 to J2.
5. Apply power to the unit and wait 60 seconds.
6. Adjust R43 clockwise and observe that the display rolls across the screen from top to bottom, adjust R43 counter-clockwise and observe that the display stops rolling then begins rolling in the opposite direction.
7. Adjust R43 to the center of the range in which the screen stops rolling in both directions.

Parabola Symmetry

1. **Power Off.** Connect scope probe to the top of R51 (between heat sinks of Q4 and Q2) and the scope ground lead to ground.



2. Set the scope for 2mS/Div and 0.5 V/Div on an AC scale. Apply power to the unit and wait 60 seconds.

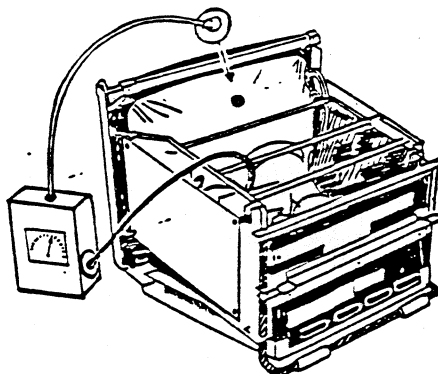
3. Adjust R114 for symmetrical parabola waveform (the points of the parabola come together).



4. Power Off. Disconnect the scope leads.

Automatic Beam Current Limiting

1. Power Off. Connect insulated milliammeter in series between the anode cap and the CRT.



WARNING! Extreme high voltage potentials exist in the flyback transformer and CRT.

2. Turn the unit on and wait 60 seconds.
3. Flood the screen with white by pressing and releasing the "BG" key, "white dot" key, and "ERASE PAGE" key.
4. Adjust R78 for 400 micro-amps on the milliammeter.

NOTE: If CRT beam current is too low the Video board may need adjustment first. Rotate R2 clockwise $\frac{3}{4}$ turn and proceed to STEP THREE. Return to this adjustment after completing the adjustments described in STEP THREE.

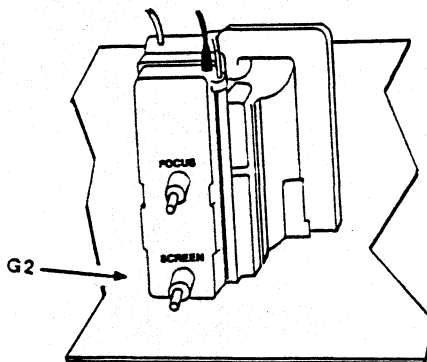
STEP THREE

The adjustable components described in this step can be found on the video module.

NOTE: It is very important that the terminal be on for the full 20 minute warm-up period before starting the alignment of the video circuitry.

Background adjustment

1. Get a "blank" screen by pressing and releasing the "BG ON", "black dot" and "ERASE PAGE" keys.



WARNING: Extremely high voltage potentials exist in the flyback transformer.

2. With the three background potentiometers on the video board in the full counter-clockwise position rotate the G2 control, on the deflection flyback transformer, clockwise until raster scan lines are barely visible.
3. Determine which color is predominant in the raster: red, green, or blue.
4. Leave the background potentiometer of the predominant color in the full counter-clockwise position. Adjust either or both of the two remaining background potentiometers for a gray raster on the screen.
5. Rotate the G2 control counter-clockwise until the raster scan lines disappear.

Gain adjust

The screen of the CRT can be flooded with selected solid colors by pressing and releasing the "BG ON" key, the key with the desired color dot, and the "ERASE PAGE" key.

1. Flood the screen with red.

Adjust R31(TC-3) or R13(AR-2) for 160-170 micro-amps on the milliammeter.

2. Flood the screen with green.

Adjust R9(TC-3) or R34(AR-2) for 180-190 micro-amps on the milliammeter.

3. Now flood the screen with blue.

Adjust R47(TC-3) or R56(AR-2) for 120-130 micro-amps on the milliammeter.

6. Flood the screen with white. Check the display for uniform white color across the screen.

NOTE: If the CRT beam current is not limited to 400 micro-amps, perform the Automatic Beam Current Limiting adjustments described in STEP TWO.

STEP FOUR

The adjustment components described in this step can be found on the deflection module.

Display Size, Centering, and Focus

1. Get a blank display on the screen. Flood the screen with white E's by pressing and releasing the "FG ON", "white dot", "ESC", "Y" and "E" keys.
2. Adjust the focus control on the flyback transformer for sharp clear characters. (See the drawing of the flyback transformer on page IV.20).
2. Flood the screen with any color.
3. Adjust R124 for a display width of 13 inches.
4. Adjust R134 for a display height of 9 3/4 inches.
5. Adjust R10 to move the display to the horizontal center of screen.
6. Adjust R138 and R139 fully counter-clockwise (from back of board).
7. Adjust R138 if display is too high on the screen.
Adjust R139 if display is too low on the screen.

NEVER ADJUST BOTH R138 AND R139 to center the display. These potentiometers cancel the effects of each other.

Pincushion and Top Corner correction

1. With a full screen of any color adjust R102 to make the sides of the display straight.
2. Adjust R120 to make the top corners of the display square.
3. Verify the adjustments performed in STEP FOUR. Screen size and character linearity are subject to change slightly, due to interaction of the circuitry.

CHAPTER V

TROUBLESHOOTING

CHAPTER V TROUBLESHOOTING

MODULAR CIRCUIT BOARD SYSTEM

Intecolor's modular circuit board design is well suited to both board level and/or component level repair. Modular circuit boards allow **faster** troubleshooting and more **cost effective** repair.

Down time can be reduced when suspected bad circuit boards are swapped with known good circuit boards to repair terminals.

Isolation of defective circuitry is easier due to the many interconnecting points.

DESCRIPTION OF TROUBLESHOOTING TABLES

The following tables offer suggestions for troubleshooting the modular analog circuitry of 3815, 3825, 3865, 3875, 8814, 8815, 8816, 8824, 8825, 8826, 8865, and 8875 Series terminals.

The tables list common **symptoms**, some of the **possible problems** that may cause the symptom, and other things to **check** to further isolate defective circuits.

The Troubleshooting Tables are organized into four sections:

SYSTEM TROUBLESHOOTING TABLE; 3800 and 8800

POWER SUPPLY; KM-3 or KM-4 and AR-2 Power Supply

DEFLECTION; KM-3 or KM-4 and AR-2

VIDEO; TC-1, AR-2, and TC-3

The **SYSTEM TROUBLESHOOTING TABLE** provides assistance when troubleshooting either 3800 or 8800 Series systems to board level. The suggestions here may help determine which analog board may cause the symptoms listed.

The board **TROUBLESHOOTING TABLES** provide more ways to help prove that the suspected board is defective. Many suggestions help isolate defective circuitry and/or components.

Troubleshooting Intecolor modular printed circuit boards may be aided by constructing extender cables. Be sure that exact pin to pin connection is observed.

Note: Cable length should be kept to a minimum.

WARNING: Be sure to place nonconductive pad (insulated for at least 40KV) under extended board.

Basic Troubleshooting Tips:

1. Carefully observe all symptoms of the problem and list them.
2. Check all fuses.
3. Check all connectors and plugs for secure fit.
4. Visually inspect all components for burns or discoloration.
5. Check for foreign objects that may have fallen into the terminal.
6. Check all circuit boards for secure installation.
7. Check Power Cord.

3800/8800 ANALOG SYSTEM TROUBLESHOOTING TABLE

SYMPTOM	POSSIBLE PROBLEM	CHECK
No Video	No High Voltage	Check for static electricity on face of CRT by placing fore-arm near face of CRT
	Power supply	Verify video source voltages. If bad, go to Power Supply troubleshooting chart.
	Video	Verify CRT filament voltage. If bad, check associated circuitry on Video and Deflection boards. With oscilloscope, verify output from video amps. If bad, go to Video troubleshooting chart
No High Voltage	Power supply	Verify output voltages at power supply connectors. If bad, go to Power Supply troubleshooting chart.
	Deflection	If power supply checks good, go to Deflection troubleshooting chart.
Discolored Letters	Screen needs degaussing	Press the Degauss Button (sometimes more than one one application is necessary)
	Video	With oscilloscope, verify TTL output from each color video amp. If one color bad, go to Video troubleshooting chart. Verify voltage regulators on video amp board. Verify video alignment.
Display distorted, Bent letters	Power Supply	Verify power supply voltages, with oscilloscope, check for ripple in DC voltages.
	Deflection	Verify deflection alignment.

SYMPTOM	POSSIBLE PROBLEM	DO THIS
Thin horizontal or vertical line in center of screen	Deflection	With oscilloscope, check vertical and horizontal oscillator output.
Video unstable	Deflection	With oscilloscope, check for ripple in low voltage regulators on deflection board.
	Power Supply	With oscilloscope, check for ripple in DC voltages from power supply.
Noise in video (wavering lines, or "snow")	Power Supply	With oscilloscope, check for double-pulsing in power supply switching transistor.
	Video	With oscilloscope, check each color amplifier output of video PCB for unsynchronized TTL pulse
	Deflection	Verify deflection alignment.

KM-3/4 POWER SUPPLY TROUBLESHOOTING TABLE

KM-3 assembly #105669

KM-4 assembly #105766

SYMPTOM	POSSIBLE PROBLEM	CHECK THIS
No output	Fuse F1 blown	Replace F1 and check Q1 for short, check R12 and R47, for increased value, if bad replace. Remove J1, J2, J3, and J7. Power unit on and check output voltages.
	Start Up voltage defective	Check collector tab of Q2 (when power is first applied) for +12 to +65 VDC. If bad, check K1, T1, BR2, and RT2.
		Check VRAW2 (when power is first applied) for +12 to +30 VDC. If bad check CR8, Q3, C30, and VR1.
		Check VREF1, if bad verify VRAW2 and/or replace VR1.
		Check U1, pin 10 for TTL low input, if bad, troubleshoot Delay Restart (U2), VRAW2 and Fault Monitor circuits.
Oscillator defective	Voltage Buss defective	Check U1, pin 11 for TTL 41.6 us square wave, if bad check U1, pin 9 for some positive voltage, if bad troubleshoot Soft-Start circuitry and Current Limiting
		Check positive leg of BR1 for positive voltage (87% of line voltage) Check negative leg of BR1 for negative voltage (87% of line), if bad check RT3 and R1
		Check collector Q2 for approx. 30 Vpp square wave, if bad, check T4 and associated components, and VRAW2.
Driver Circuit defective		With F1 removed and floating ground oscilloscope, (use Delta ground) check base of Q1 for switching signal if bad check Q12 and associated circuits.
		Check collector of Q1 for high positive flyback pulses, if bad check Q1, and T2.

SYMPTOM	POSSIBLE PROBLEM	CHECK
Unit Blows F1 with load on	Q1 defective	Check Q1 for shorts (Always check Q1 if F1 blows). Replace F1 and/or Q1, disconnect J1 and J2, and check output voltages
	Driver Circuitry defective	Check CR5, R4, and R16.
	Soft Start defective	Check Q11, Q13, and associated circuits.
	Current Limiting defective	Check C8, and CR1
Unit Blows F1 with all loads removed	Q1 defective	Check Q1 for shorts. Always check Q1 if F1 blows.
	Driver Circuitry defective	Check CR5, R4, and R16.
	Output Voltage circuitry defective	Check for near short to ground at J1, pins 1, 3, J2, pin 8, and CR10 anode.
	Oscillator defective	Check U1, pin 11, for less than 50% positive duty cycle square wave signal.
Unit shuts down with loads on	Defective Load	Remove J1 and J2, Check output voltage.
	Driver Circuitry defective	Check R12, R61, Q12, and CR20 for open.
	Reference Voltage regulators defective	Check VR1, VR2, VR3, and VR4.
	Output Voltage circuitry defective	Check +5 VDC circuit. Check other output circuitry.

SYMPTOM	POSSIBLE PROBLEM	CHECK
Unit shuts down with loads removed	Reference Voltage circuitry defective	Check CR8, VR1, VR2, VR3, and VR4.
	Output Voltage circuitry defective	Check +16 VDC output and +5 VDC output circuitry and other output circuits.
	Current Limiting circuitry defective	Check CR1, C8, and R51.
Power Supply causes noise on screen	HSYNC circuitry defective	With W1 removed check collector of Q4 for HSYNC pulse.

AR-2 POWER SUPPLY
TROUBLESHOOTING TABLE
AR-2 Assembly # 105684

SYMPTOM	POSSIBLE PROBLEM	CHECK
No output	Fuse F1 blown	Replace F1 and check Q1 for short, check R12 and R13, if bad replace. Remove J1, J2, J3, J7, and J8. Power unit on and check output voltages.
	Start Up Voltage defective	Check collector tab of Q2 (when power is first applied) for +12 to +65 VDC. If bad, check K1, T1, BR2, and RT2
		Check VRAW2 (when power is first applied) for +12 to +30 VDC. If bad check CR8, Q3, C30, and VR1
		Check VREF1, if bad verify VRAW2 and/or replace VR1
		Check U1, pin 10 for TTL low input, if bad troubleshoot Delay Restart (U2), VRAW2 and Fault Monitor circuits
	Oscillator defective	Check U1, pin 11 for TTL 41.6 uS square wave, if bad check U1, pin 9 for some positive voltage, if bad troubleshoot Soft-Start circuitry and Current Limiting
	Voltage Bus defective	Check positive leg of BR1 for positive voltage (approx. 87% of line voltage) Check negative leg of BR1 for negative voltage (approx. 87% of line), if bad check RT3 and R1
	Driver Circuit defective	Check collector Q2 for approx. 30 Vpp square wave, if bad, check T4 and associated components, and VRAW2
		With F1 removed and floating ground oscilloscope, (use Delta ground) check base of Q1 for switching signal if bad check Q12 and associated circuits

SYMPTOM	POSSIBLE PROBLEM	CHECK
No Output (Cont.)		Check collector of Q1 for high positive flyback pulses, if bad check Q1, and T2
Unit Blows F1 with load on	Q1 defective	Check Q1 for shorts Always check Q1 if F1 blows. Replace F1 and/or Q1, disconnect J1, J2, J3, and J8 and check output voltages
	Driver Circuitry defective	Check CR5, R4, and R16
	Soft Start defective	Check Q11, Q13, and associated circuits
	Current Limiting defective	Check C8, and CR1
Unit Blows F1 with all loads removed	Q1 defective	Check Q1 for shorts Always check Q1 if F1 blows
	Driver Circuitry defective	Check CR5, R4, and R16
	Output Voltage circuitry defective	Check for near short to ground at J1, pins 1, 3, J2, pin 8, and CR10 anode
	Oscillator defective	Check U1, pin 11 square wave signal for less than 50% positive duty cycle,
Unit shuts down with load on	Defective Load	Remove J1, J2, J3, and J8, check output voltages
	Driver Circuitry defective	Check R12, R61, Q12, and CR20 for open
	Reference Voltage regulators defective	Check VR1, VR2, VR3, and VR4
	Output Voltage circuitry defective	Check +5 VDC circuit Check other output circuitry

Intecolor

SYMPTOM	POSSIBLE PROBLEM	CHECK
Unit shuts down with loads removed	Reference Voltage circuitry defective	Check CR8, VR1, VR2, VR3, and VR4
	Output Voltage circuitry defective	Check +16 VDC output and +5 VDC output circuitry and other output circuits
	Current Limiting circuitry defective	Check CR1, C8, and zero ohm R51
Power Supply causes noise	HSYNC circuitry defective	With W-1 removed check collector of Q4 for HSYNC pulse
		Check PLL circuitry

KM-3/4 DEFLECTION
TROUBLESHOOTING TABLE
KM-3 Assembly #103302
KM-4 Assembly #105763

SYMPTOM	POSSIBLE PROBLEM	CHECK
No video	No High Voltage	Check for 25KV at anode of CRT. If incorrect, Go to "No High Voltage" symptom
	No Filament voltage	Check for approx 20 VAC at J8, pin 7
	Defective Logic	Verify Logic Board
	Defective Video	Go to Video troubleshooting and/or Alignment
Thin horizontal line in center of CRT screen	Defective Vertical Oscillator	Check Vertical Oscillator output ramp Emitter Q13
	Defective Vertical Deflection	Check for +45 VDC at R74. If bad check C2 and CR1
		Check for signal at collector Q14
Bent Letters	Defective Pincushion correction	Check for parabola at collector Q18
	Defective Horizontal Voltage Regulator	Check for 0VDC at U3 pin 2 Check Q8, Q9, Q10 for short or open
	Jumper misplaced	Check Jumper configuration table
Video Rolls Vertically on Screen	Vertical Sync Defective	Check collector of Q12 for Sync pulse
	Vertical Oscillator Defective	Check for consistent ramp signal output at U2, pin 6
Video Rolls Across Screen Side to Side	Horizontal Sync Defective	Check collector of Q20 for Sync pulse
	Defective Retrace Pulse	Check for open R98 Check for shorted C83, CR40 or CR41
	Defective Horizontal Oscillator	Check U1, pin 9 for +6 VDC, U1, pin 4 for square wave signal

SYMPTOM	POSSIBLE PROBLEM	CHECK
No High Voltage	Defective Horizontal oscillator	Check +12 VDC Check U1, pin 4 for square wave signal
	Defective Base Drive	Check collector Q22 for Base Drive Pulse
	Defective Power Supply	Verify Power Supply
	Defective Horizontal Deflection	With J7 disconnected, check J7, pin 3 for 100 VDC +/-10 VDC
	Defective Voltage Regulator	Check U3 and associated circuitry
	Defective Q23 or CR42	Check components for open/short
	NOTE: If Q23 or CR42 are found short, disconnect J5 and verify that power supply operates properly.	
Thin vertical line in center of screen	Defective Horizontal Deflection	Check for open in jumper W4, L4, L5, R106 or yoke of CRT
Noise in Video	Ripple in +12 VDC	Check +16 VDC Input from Power Supply
	Ripple in -12 VDC	Check +12 VDC Regulator
		Check -12 VDC Input from Power Supply

**AR-2 DEFLECTION
TROUBLESHOOTING TABLE**
AR-2 Assembly #105159

SYMPTOM	POSSIBLE PROBLEM	CHECK
No video	No High Voltage	Check for 25KV at anode of CRT. If incorrect, Go to "No High Voltage" symptom
	No Filament voltage	Check for approx 20 VAC at J4, pin 4 if good go to Video troubleshooting
	Defective Logic	Verify Logic Board inputs to video board
	Defective Video	Go to Video troubleshooting and/or Alignment
Thin horizontal line in center of CRT screen	Defective Vertical Oscillator	Check Vertical Oscillator output ramp U3, pin 5
	Defective Vertical Deflection	Check +28 VDC from power supply
Bent Letters	Defective Pincushion correction	Check for parabola at U5, pin 7
	Defective Horizontal Voltage Regulator	Check emitter of Q2 for parabola signal on B+ voltage
Video Rolls Vertically on Screen	Vertical Sync defective	Check collector of Q22 for Sync pulse
	Vertical Oscillator Defective	Check for ramp signal at U3, pin 2
Video Rolls Across Screen Side to Side	Horizontal Sync Defective	Check U1, pin 1 for HSYNC pulse
	Horizontal centering defective	Check U2, pin 5 for a 4us TTL pulse
	Defective Retrace Pulse	Check U3, pin 13 for a 3 Vpp ramp with fast rise and slow fall time

SYMPTOM	POSSIBLE PROBLEM	CHECK
No High Voltage	X-ray protect	Check U5 pin 1 for -12 VDC, if +12 VDC X-ray circuit is shutting off hor. oscillator. See Tips on Troubleshooting AR-2 deflection at the end of this chart
	Horizontal protect	Check base of Q10 for positive bias voltage
	Defective Power Supply	Verify Power Supply
	Defective Voltage Regulator	Check +12 VDC U3, pin 22, and pin 11
	Defective Q8 or CR4	Check components for open/short

NOTE: If Q8 or CR4 are found short, disconnect J5 and verify that power supply operates properly.

Noise in Video	Ripple in +12 VDC	Check +16 VDC Input from Power Supply
		Check +12 VDC Regulator
	Ripple in -12 VDC	Check -12 VDC Input from Power Supply

Tips on Troubleshooting the AR-2 Deflection.

When operating properly, a positive voltage at U3, pin 8, from the X-Ray protect circuitry disables the horizontal oscillator output from U3, pin 9, whenever the high voltage exceeds 29KV.

Damage to other circuitry may result if the X-Ray protect circuitry is modified (disabled). However, the high voltage circuitry may be disabled by lifting one end of Resistor R30 (see PCB Silkscreen in Appendix D).

With the high voltage generation circuitry disabled, the voltage from the X-Ray protect circuitry to U3, pin 8, should be -12 vdc. If this voltage is positive when the HV is disabled, troubleshoot the X-Ray protect circuitry.

Check the components in the HV circuitry if the X-Ray protect circuits are functioning properly.

TC-1 VIDEO AMPLIFIER
TROUBLESHOOTING TABLE
TC-1 Assembly #105112

SYMPTOM	POSSIBLE PROBLEM	CHECK
Discolored characters	No output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "No output of amp"
	Weak output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "Weak output of amp"
	VR1 defective	Check +5 VDC output of VR1 (also check for ripple)
Full screen of white rastors	+60 VDC supply low	Disconnect J1 check +60 VDC from power supply
	Shorted U1	Check U1 inputs for short to ground Check U1 outputs for TTL square wave, if +5 VDC (no square wave) output, replace U1
	Defective G2 voltage	Check R50 for open
Red, Green, or Blue rastors	Shorted component or components in affected color	Check components in Amplifier and Low Level Video Control circuits for short to ground
	+5 VDC bad	Check for short at output of VR1
	Push pull amp defective	Check components in upper part of push-pull amplifier circuitry
No video	Defective logic	Check for TTL square wave at pins 1, 3, and 5 of J2
	+12 VDC defective	Disconnect J1 and check +12 VDC from power supply
	Defective U1	Check output pins for TTL square wave
	Defective Tube Bias or filament voltages	Check J1; pin 7, for 20 +/- 6 VAC heater voltage, pin 4 for -100 VDC G1 voltage

SYMPTOM	POSSIBLE PROBLEM	CHECK
Weak video	Defective logic	Check J2 pin 9, for +5 VDC (no INT BIT)
	Defective Intensity Bit Control circuitry	Check Q11 and Q12 and associated circuitry
	Defective ABL circuitry	With black screen check J1 pin 3 for some voltage less than -7.5 volts (CR24 begins to conduct at -7.5 VDC) Check Q16, Q15 and associated circuits
No output of amp	Defective Low Level Video Control circuitry	Check for TTL square wave through Low Level Video Control circuits
	Defective "control" transistor	Check for open collector to emitter Q3 Green, Q6 Red, Q9 Blue
	VR1 defective	Check +5 VDC output of VR1.
	Defective Gain Adjust amp	Check Gain amp Q12 Green, Q13 Red Q14 Blue and associated circuits
	Defective Push-pull amp	Check transistor Q1, Q2 Green, Q4, Q5 Red, Q7, Q8 Blue and associated circuitry
	Defective +12 VDC supply voltage	Check +12 VDC from power supply
Weak output of amp	Shorted diode	Check CR14 Green, CR15 Red, CR16 Blue
	Defective Low Level Video Control circuitry	Check resistors between emitter of "control" transistor and NAND gates for opens
	Defective "control" transistor	Replace transistor Q3 Green, Q6 Red, Q9 Blue
	VR1 defective	Check +5 VDC output of VR1
	Defective Gain Control amp	Rotate Gain Control potentiometer CW (from rear of board) and check base of "control" transistor Q3 Green, Q6 Red, Q9 Blue for

SYMPTOM	POSSIBLE PROBLEM	CHECK
Weak output of amp. (cont.)		+6 VDC (+/- 1.5 VDC)
	Increased impedance in "control" amp supply voltage line	Check R1, L4 Green, R16, L5 Red, R31, L6 Blue
	Defective +12 VDC	Check +12 VDC from power supply
	Jumpers	Jumpers must be installed
No ABL	+5 VDC bad	Check +5 VDC from VR1
	ABL circuitry defective on deflection board	Check J1, pin 3 for voltage greater than -7.5 VDC with full white screen

**AR-2 VIDEO AMPLIFIER
TROUBLESHOOTING TABLE**
AR-2 Assembly #105199

SYMPTOM	POSSIBLE PROBLEM	CHECK
Discolored characters	No output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "No output of amp"
	Weak output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "Weak output of amp"
	VR1 defective	Check +5 VDC output of VR1 (also check for ripple)
Full screen of white rastors	+90 VDC supply low	Disconnect J3 and J4, check +90 VDC from power supply
	Defective G2 VDC	Check R15 for open
Red, Green, or Blue rastors	Shorted component/ components in affected color	Check components in Amplifier and Low Level Video Control circuits for short to ground
	Open component/ components in affected color	Check components in background circuit and between its output and collector of: Q18 Green, Q10 Red, Q26 Blue
		Check components in upper part of push-pull amplifier circuitry
No video	Defective logic	Check for TTL square wave at pins 1, 3, and 5 of J1
	+12 VDC defective	Disconnect J3 and J4, check +12 VDC from power supply
	Defective Tube Bias and filament voltages	Check J4; pin 4, for 20 +/- 6 VAC heater voltage, pin 3 for -100 VDC
Weak video	Defective logic	Check J1 pin 9, for +5 VDC (no INT BIT)
	Defective Intensity Bit Control circuitry	Check Q7 and Q8 and associated circuitry

SYMPTOM	POSSIBLE PROBLEM	CHECK
Weak Video (cont.)	Defective Vertical Retrace Blanking circuitry	Check Q1, Q2, Q29, emitter to base, for short Check J4 pin 2, for blanking pulse
	Defective ABL circuitry	With black screen check J4 pin 6 for some voltage less than -7.5 volts (CR24 begins to conduct at -7.5 VDC) Check Q3, Q4 and associated circuits
No output of amp.	Defective "control" transistor	Check for open, collector to emitter, Q18 Green, Q10 Red, Q26 Blue
	VR1 defective	Check +5 VDC output of VR1.
	Defective Gain Adjust amp	Check Gain amp Q16 Green, Q8 Red Q24 Blue and associated circuits
	Defective Push-pull amp	Check transistor Q19, Q20 Green, Q11, Q12 Red, Q27, Q28, Blue and associated circuitry
	Defective +12 VDC supply voltage	Check +12 VDC from power supply
Weak output of amp	Defective "control" transistor	Replace transistor Q18 Green, Q10 Red, Q26 Blue
	VR1 defective	Check +5 VDC output of VR1
	Defective Gain Control amp	Rotate Gain Control potentiometers CW (from rear of board) and check base of "control" transistor Q18 Green, Q10 Red, Q26 Blue for +6 VDC (+/- 1.5 VDC)
	Increased impedance in "control" amp supply voltage line	Check components in "control" amp supply line
	Defective +12 VDC	Check +12 VDC from power supply

TC-3 VIDEO AMPLIFIER
TROUBLESHOOTING TABLE
TC-3 Assembly #105202

SYMPTOM	POSSIBLE PROBLEM	CHECK
Discolored characters	No output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "No output of amp"
	Weak output from one or more video amps	Determine which amp is defective by checking full screen floods of Red, Green, and Blue. Go to "Weak output of amp"
	VR1 defective	Check +5 VDC output of VR1 (also check for ripple)
Full screen of white rastors	+90 VDC supply low	Disconnect J3 and J4, check +90 VDC from power supply
	Shorted U1	Check U1 inputs for short to ground. If short replace U1
		Check U1 outputs for TTL square wave, if +5 VDC (no square wave) output, replace U1
Red, Green, or Blue rastors	Defective G2 voltage	Check R67 for open
	Shorted component/ components in affected color	Check components in Amplifier and Low Level Video Control circuits for short to ground
		Check for short at output of VR1
	Open component/ components in affected color	Check components in background circuit and between its output and collector of: Q5 Green, Q13 Red, Q19 Blue
		Check components in upper part of push-pull amplifier circuitry
No video	Defective logic	Check for TTL square wave at pins 1, 3, and 5 of J1
	+12 VDC defective	Disconnect J3 and J4, check +12 VDC from power supply

SYMPTOM	POSSIBLE PROBLEM	CHECK
No video (cont.)	Defective U1	Check output pins for TTL square wave
	Defective Tube Bias and filament voltages	Check J4; pin 4, for 20 +/- 6 VAC heater voltage, pin 3 for -100 VDC
Weak video	Defective logic	Check J1 pin 9, for +5 VDC (no INT BIT)
	Defective Intensity Bit Control circuitry	Check Q7 and Q8 and associated circuitry
	Defective Vertical Retrace Blanking circuitry	Check Q1, Q22, Q22, emitter to base, for short
		Check J4 pin 2, for blanking pulse
	Defective ABL circuitry	With black screen check J4 pin 6 for some voltage less than -7.5 volts (CR24 begins to conduct at -7.5 VDC)
No output of amp		Check Q24, Q23 and associated circuits
	Defective Low Level Video Control circuitry	Check for TTL square wave through Low Level Video Control circuits
	Defective "control" transistor	Check for open collector to emitter Q5 Green, Q13 Red, Q19 Blue
	VR1 defective	Check +5 VDC output of VR1.
	Defective Gain Adjust amp	Check Gain amp Q4 Green, Q12 Red Q18 Blue and associated circuits
	Defective Push-pull amp	Check transistor Q3, Q6 Green, Q11, Q14 Red, Q17, Q20 Blue and associated circuitry
	Defective +12 VDC supply voltage	Check +12 VDC from power supply
	Shorted diode	Check CR2 Green, CR10 Red, CR16 Blue

SYMPTOM	POSSIBLE PROBLEM	CHECK
Weak output of amp	Defective Low Level Video Control circuitry	Check resistors between emitter of "control" transistor and NAND gates for opens
	Defective "control" transistor	Replace transistor Q5 Green, Q13 Red, Q19 Blue
	VR1 defective	Check +5 VDC output of VR1
	Defective Gain Control amp	Rotate Gain Control potentiometer CW (from rear of board) and check base of "control" transistor Q5 Green, Q13 Red, Q19 Blue for +6 VDC (+/- 1.5 VDC)
	Increased impedance in "control" amp supply voltage line	Check R6, L1 Green, R29, L3 Red, R46, L5 Blue
	Defective +12 VDC	Check +12 VDC from power supply

CHAPTER VI

CIRCUIT DESCRIPTIONS

CHAPTER VI
CIRCUIT DESCRIPTION
3800/8800 MODULAR ANALOG BOARDS

Section Content:

This section describes each analog modular circuit board that is used by 3815, 3825, 3865, 3875, 8814, 8815, 8816, 8824, 8825, 8826, 8865, and 8875 terminals.

The section is in three parts.

The first part, THE AUTO-RANGING POWER SUPPLY.

KM-3	page VI.3
KM-4	page VI.3
AR-2	page VI.12

The second part, THE DEFLECTION BOARD.

KM-3	page VI.24
KM-4	page VI.24
AR-2	page VI.33

The third part, THE VIDEO BOARD.

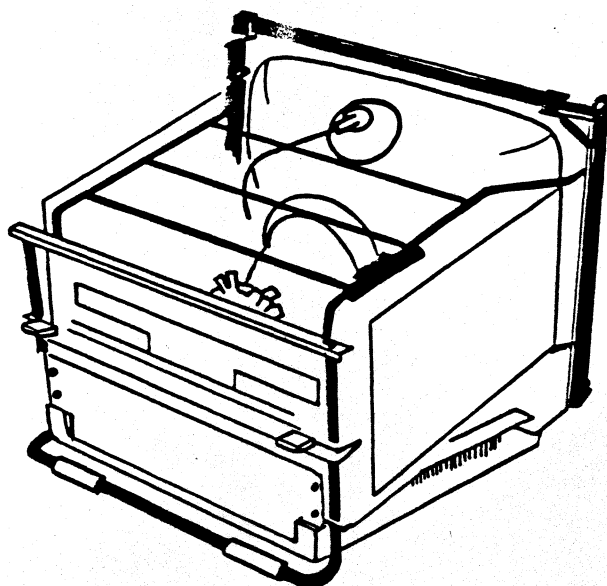
TC-1	page VI.48
AR-2	page VI.54
TC-3	page VI.61

Each detailed circuit Description is divided into blocks of circuitry. The first paragraph of each "Block" describes the purpose of the circuitry. The paragraphs that follow describe in detail the functions of the circuitry. A **Functional Block Diagram** is shown at the beginning of each circuit description. Block diagram drawings for all modular analog boards are also available in appendix E, beginning on page E-1.

THE AUTO-RANGING POWER SUPPLY BOARD

The circuitry of the Power Supply board converts input line AC voltage into many stable DC output voltages. Intecolor's patented "auto-ranging" power supplies utilize "Flyback" topology switching technology to provide the regulated output voltages. In these power supplies, stable output voltages are maintained with varying input line voltages and frequencies, without changing any switches or jumpers.

The Power Supply board is located on the right side when looking at the rear of the unit.



Identification of the Auto-ranging Power Supply boards and relative schematics are shown below.

		SCHEMATIC	BOARD
3800	KM-3 Power Supply	# 105667	# 105669
3800	KM-4 Power Supply	# 105764	# 105766
8800	AR-2 Power Supply	# 105682	# 105684

KM-3 and KM-4 POWER SUPPLIES

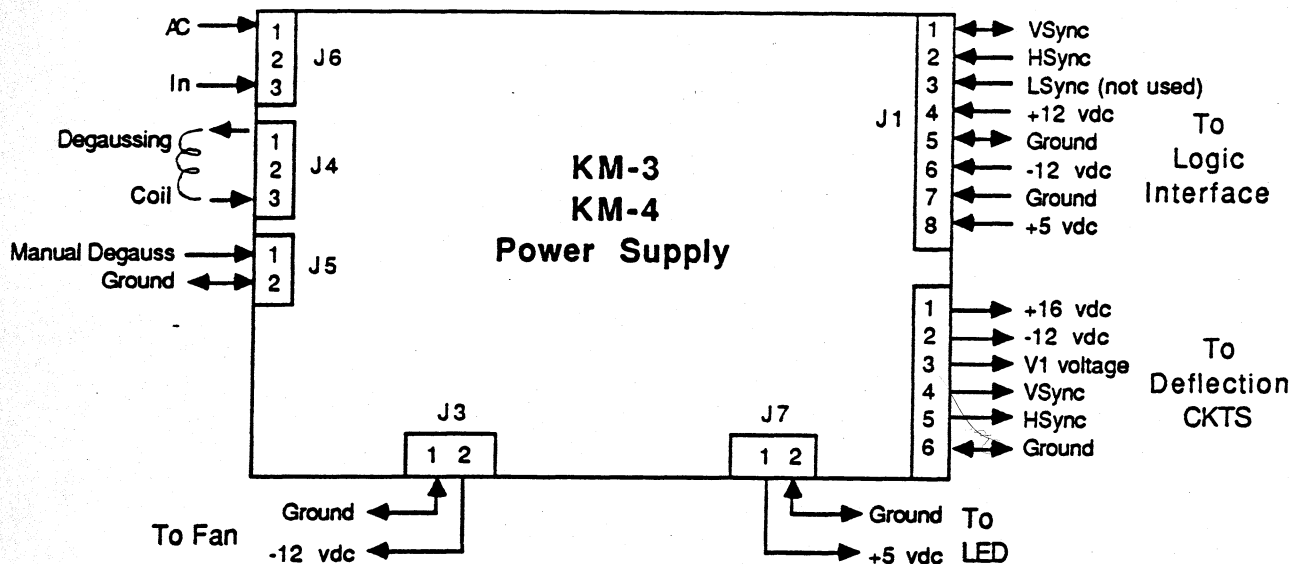
Refer to schematic drawing #105667 rev 2 or later for the KM-3 power supply.

Refer to schematic drawing #105764 rev 2 or later for the KM-4 power supply.

The KM-3 and KM-4 power supplies are Intecolor's first generation of "auto-ranging" power supplies. The power supplies automatically adjust for line voltage variations of 86 to 250 VAC, and line frequency variations of 40 to 70 Hz while still maintaining stable output voltages. This enables the power supplies to be used anywhere in the world without requiring changes in jumpers or switches to accommodate different line voltages and frequencies.

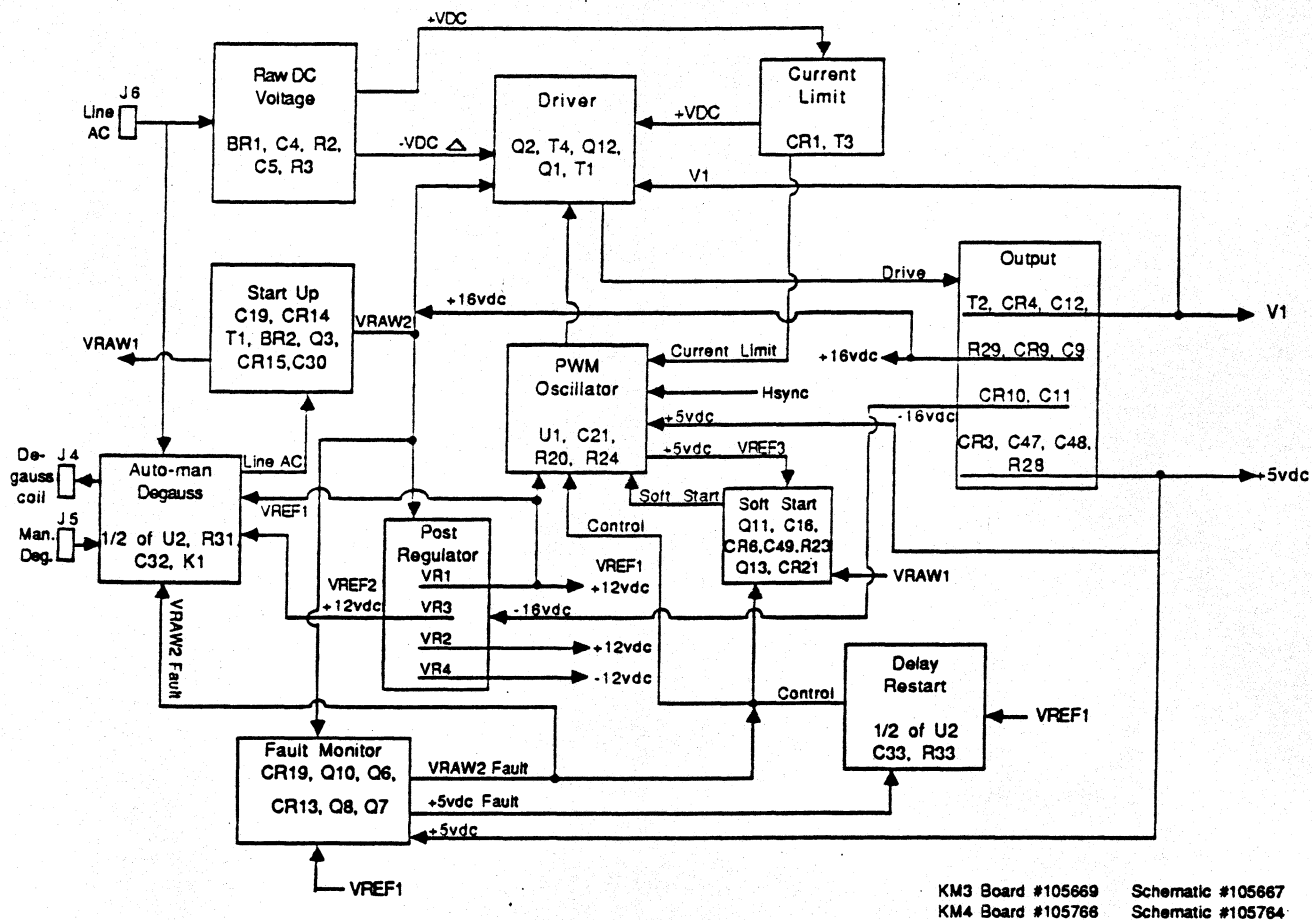
Circuitry and physical lay-out of the KM-3 and KM-4 boards are similar. The KM-3 power supply is modified from original design with in-rush current protecting thermistors added to the voltage bus circuitry. The KM-4 is the latest revision of the KM-3 with provision for installing these thermistors in the printed circuit board. The following descriptions are true for both power supplies.

Input and Output wiring:



BLOCK DIAGRAM

KM-3/4 Power Supply



Circuit Description:

Start Up Voltage section contains a conventional linear type power supply with a specially designed transformer to operate over a broad range of line frequencies and voltages. This circuitry provides the switching regulator with an operating voltage for a short period of time when power is first applied to the unit or the **Auto/Manual Degaussing** circuit is activated. Circuitry consists of T1, BR2, C19, Q3, and associated components.

Line AC is input at J6, to the Raw DC Voltage circuits, and through relay K1 to the Start Up Voltage circuits. Current flows through normally closed contacts of relay K1 (pin 7 and 6), transformer T1, resistor RT2, and back to J6. T1 steps down the voltage, which is then rectified into a DC voltage (VRAW1) by BR2 and filtered by capacitor C19. VRAW1 typically ranges from +12 VDC to +65 VDC depending on the line voltage.

VRAW1 is used by the Soft Start circuitry to detect the presence of high line voltage.

Transistor Q3, resistor R26, and 30 volt zener diode CR14, form a series-pass regulator to limit the output voltage (VRAW2), to +30 VDC. VRAW2 at this point, is an intermediate voltage supplied to the Post Regulator section and Switching circuits during start up. VRAW2 is also an input to the Fault Monitor section.

Shortly after the power supply comes up to full operating potential, K1 opens the path for current to flow through T1. By this time, VRAW2 is provided by the power supply itself through diode CR8. Capacitor C30 provides a smooth transition from the T1 VRAW2 and the VRAW2 provided by the power supply.

Diode CR15 protects Q3 from damage when VRAW2 is provided by the power supply. CR8 prevents the VRAW2, provided by T1, from supplying the other regulators in the Post Regulator section.

Line voltages around 250 VAC will damage T1 if K1 fails to open at its pins 6 and 7. RT2 is a positive coefficient resistor that protects T1 when the line voltage is high and K1 fails. If line voltage is 250 VAC and K1 fails, current flow causes RT2 to heat up and open after about 30 seconds. RT2 should never activate under normal conditions. Should RT2 activate, five minutes cooling time should reset RT2.

Raw DC Voltage circuitry converts the AC line voltage into unregulated DC voltages for the Switching Circuits main switching transistor and transformer. Circuitry consists of Y-capacitors C1, C2, and C6, X-capacitor C3, full wave bridge rectifier BR1, and associated components.

Line AC is input through J6 and rectified by full wave bridge BR1. The resulting DC voltage is filtered by capacitors C4 and C5, while resistors R2 and R3 provide safety bleeder current. Positive DC output (across R3) provides current to the main Switcher through F1.

WARNING: The negative side of the output (Delta Ground) floats with respect to chassis ground. Use extreme caution when making measurements in this circuitry.

The special X and Y capacitors, C1, C2, C3, and C6, form part of an EMI/RFI filter. These capacitors must meet IEC standards, and must be replaced with the same approved type capacitors. Additional filtering, in the form of the line filter, is necessary to complete the EMI/RFI filtering to meet FCC requirements.

All KM-4 boards and KM-3 boards Revision 3 and higher have negative coefficient thermistors installed in the AC input lines to provide in-rush current protection. As these thermistors heat up their resistance decreases.

Delay-Restart circuitry delays the output of the Pulse Width Modulated Oscillator for 3 to 5 seconds and discharges the Soft Start capacitors. One half of U2, a 556 IC dual timer, and associated circuitry provides this function.

When VREF1 reaches approximately +5 VDC, U2 starts to operate. The time delay for this half of U2 is determined by resistor R33 and capacitor C33. U2, pin 5 is high approximately 3 to 5 seconds.

The high at U2, pin 5 is at U1, pin 10 and makes sure that U1 remains shutdown long enough for VREF1 to reach a stable +12 VDC output. The high from pin 5 also biases transistor Q11 on to discharge the Soft Start capacitors.

When the Delay Restart circuits time out (3 to 5 seconds), U1, pin 10 goes low and the power supply begins providing the VRAW2 voltage to the Post Regulator section.

The Delay Restart circuitry can be forced to start over if the Fault Monitor circuitry detects a drop in the +5 VDC from the power supply output.

Auto/Manual Degaussing circuitry allows degaussing of the CRT and prevents K1 from interrupting current flow through T1 prematurely. Each time power is turned on or the manual degauss button is pressed, the screen of the CRT is degaussed. Circuitry consists of 1/2 of U2, relay K1, and associated circuitry.

When VREF1 reaches approximately +5 VDC, U2 starts to operate. The time delay for this half of U2 is determined by resistor R31 and capacitor C32. U2, pin 9 is high approximately 6 to 9 seconds. During this time, AC current flows through the contacts of relay K1 and a coil surrounding the face of the CRT.

VREF2 is produced by the power supply after the Delay Restart circuits have timed out (3 to 5 seconds).

The high from U2, pin 9 biases transistor Q9 on. When Q9 conducts, Q5 is biased off and K1 cannot energize. While K1 is de-energized, current flows through T1 and the degaussing coil of the CRT. RT1 allows a large initial current to flow through the degaussing coil. As RT1 heats up, its resistance increases, thus gradually reducing the current flow through the degaussing coil to provide proper degaussing action.

Notice that the Delay Restart circuitry allows the power supply to start producing output voltages a few seconds before the current through T1 is interrupted. T1 generated VRAW2 is maintained briefly, allowing time for the power supply output voltages to stabilize.

The Auto/Manual Degaussing circuits can be forced to start over by the Fault Monitor circuits or a manual degaussing input. The Fault Monitor or the manual degaussing input will short pin 1 of J5 to ground. Capacitor C34 discharges and passes a low pulse to U2, pin 8. A low on pin 8 resets the Auto/Manual Degaussing side of U2. U2, pin 9 goes high and that side of the timer starts over again.

Diode CR12, across the coil of K1, protects Q5 from the kick-back voltage generated by the collapsing field around the core of K1 when Q5 turns off.

Soft Start circuitry prevents the power supply from starting too quickly and destroying itself. Circuitry consists of diode CR6, transistors Q11 and Q13, and associated circuitry.

When line voltage is larger than 180 VAC, a VRAW1 greater than +39 VDC is generated by BR2. Zener diode CR21 is sufficiently reverse biased to bias Q13 on and C49 is in the circuit.

The high provided by U2, pin 5, is on the base of Q11, biasing it on. Q11 discharges capacitor C16 (and C49 when line voltage is large enough) and forward biases CR6 to hold down pin 9 of U1.

When Q11 is biased off, by U2, pin 5 going low, C16 (and C49) charge toward VREF3 (+5 VDC) provided by U1, pin 16, through resistor R23. C16 (and C49) charging toward +5 VDC gradually decrease forward bias on CR6 and allows U1, pin 9 voltage to rise.

U1 contains a pulse width modulator (PWM) circuit. The voltage on pin 9 controls the width of the PWM output pulses; lower voltage results in narrower pulses. By forcing pin 9 low and allowing its voltage to rise slowly, power supply soft start is performed.

Oscillator circuitry provides the Switching circuitry with a regulated pulse width modulated square-wave. Circuitry consists of U1 and associated components.

U1 is a special voltage controlled, pulse width modulated, oscillator IC. Capacitor C21 and the resistor selected by jumper W4 (R17, R18, or R9) provide an RC network for the oscillator in U1. When VREF1 is input to U1, pin 15 a ramp signal is developed at pin 7. VREF3 is generated by U1 and is a highly stable +5 VDC output at pin 16.

The +5 VDC power supply output is used as feedback through resistor R57, adjusted by R24, and input to U1, pin 1. VREF3 is used as a reference voltage through resistor R20 and input to U1, pin 2. The voltage on U1, pin 1 is adjusted to set the +5 VDC power supply output.

Power supply regulation is as follows:

An internal error amplifier compares voltages on U1, pins 1 and 2, and outputs an error signal that can be observed at pin 9. This error voltage can be over-ridden by either the **Current Limiting** circuitry input at pin 4, or **Soft Start** circuitry connected to pin 9.

If the +5 VDC power supply output voltage tries to increase, such as when current demands decrease. The feedback voltage to U1, pin 1 rises higher than pin 2, and the error voltage at pin 9 decreases.

When the ramp signal at U1, pin 7, exceeds the error voltage at pin 9, the output of the PWM comparator is disabled. The width of positive pulses output from U1, pin 11 are decreased and the power supply reduces its output.

If the +5 VDC power supply output voltage tries to decrease, such as when current demands increase. The feedback voltage to U1, pin 1 drops lower than pin 2, and the error voltage at pin 9 increases.

When the error voltage exceeds the ramp voltage, the output of the PWM comparator is enabled. The width of positive pulses output from U1, pin 11 are increased and the power supply output voltages increase.

A high at U1, pin 10 disables the output of the PWM.

Switching circuitry provides a controlled AC voltage for the power supply **Output** section. Circuitry consists of transistors Q2, Q12 and Q1, transformers T4 and T2, and associated components.

The Oscillator output is at the base of Q2. During initial start-up of the switching circuitry, VRAW2 (generated by T1) provides supply voltage for T4 and Q2. Once the power supply provides output voltages, V1 is the primary source voltage for T4 and Q2. Diode CR16 prevents V1 voltage from entering VRAW2 while diode CR2 prevents VRAW2 from powering V1 circuits.

Positive pulses bias Q2 on, current flows into pin 1 of T4 and a positive voltage is applied to T4, pin 6. Transistor Q1 is biased on and current flows from Delta Ground through Q1 and the primary of T2. A positive voltage is applied to pin 1 of T2. Polarity dots drawn on the schematic show that the secondary output diodes are reverse biased and no energy is transferred to the secondaries. Energy is stored in the core of T2 in the form of a magnetic field.

When Q2 is switched off by the oscillator output, Q1 is biased off. The collapsing magnetic field induces a voltage in the secondary windings which forward biases the secondary diodes and energy is drained from T2 into the output capacitors.

In a switching circuit where a transistor is required to turn-off an inductive load, the collector is subjected to current and voltage stresses at the same time. Capacitor C7, resistors R4 and R16, and diode CR5 form a turn-off "snubber" to protect Q1 from induced stress. As Q1 turns off, the T1 primary inductor current begins to flow through C7 and CR5, charging C7. Once the inductor current subsides, R4 and R16 discharge C7 so that the "snubber" is ready for the next cycle of the switching circuitry.

Besides snubbing the turn-off current away from Q1 it is also necessary to turn Q1 off quickly to minimize the peak power dissipated.

When Q2 is biased on, positive current flows into the base of Q1, out the emitter and back to pin 5 of T4 through resistor R61, capacitor C10 and diode CR20. This positive current turns Q1 on and charges C10 to a value determined by R61.

When Q2 is biased off, transistor Q12 is biased on, placing C10 between the emitter and base of Q1. The charge on C10 reverse biases Q1 base to emitter and ensures that it turns off quickly.

Resistor R12 aids in turning off Q1 while capacitor C17 helps turn Q12 on quickly.

Diode CR17 and resistor R11 control the shape of the turn-off pulse delivered to the base of Q1.

Note:

The schematic shows that Q1 transistor may be either a BUX88 or MJ8505. The MJ8505 transistor is preferred for reliable long term circuit operation. The BUX88 transistor will run typically 10 degrees hotter than the MJ8505, which impacts long-term reliability.

Intecolor checks the Beta of all the transistors installed as Q1. Transistors with Beta less than 18 are preferred, however some power supplies have been modified to accept Q1 transistors with Beta up to 25. The modification is in the **Switching** circuitry; resistor R49 may be changed from a 56 ohm to a 120 ohm resistor.

Output circuits rectify and filter the AC voltage provided by the **Switching** circuitry to generate the output voltages. Circuitry consists of, the secondaries of T2, diodes CR9, CR10, CR3 and CR4, and associated components.

CR9 allows positive pulses to charge C9 and produce the VRAW2 voltage and +16 VDC output at J1, pin 1.

CR10 allows negative pulses to charge C11 and produce the -16 VDC output to the **Post Regulator** section.

CR3 is a paralleled Schottky diode pair. CR3 allows positive pulses to charge capacitors C47 and C48 and produce the +5 VDC that is used as feedback for regulation, monitored by the **Fault Detect** circuits and is output to J2, pin 8. Since the +5 VDC is used for regulation, R28 provides a minimal load if the external load is removed.

CR4 allows positive pulses to charge capacitor C12 and produce the high V1 voltage (+70 - +90 VDC) that is output to J1, pin 3 and the **Switching** circuit. Since V1 is used as a supply voltage for a transistor in the **Switching** circuits, resistor R29 provides a minimal load if the external load is removed. Jumper W3 allows a selection of three different V1 values.

Post Regulator circuitry generates regulated low voltage outputs to various circuits on the board and provide +12 VDC and -12 VDC outputs to the output connectors on the board. Circuitry consists of regulators VR1, VR2, VR3, and VR4 with associated components.

VRAW2 provided by the **Start Up Voltage** circuitry or the power supply **Output** section provides supply voltage for VR1. VR1 generates the stable +12 VDC VREF1.

Diode CR8 prevents the VRAW2 generated by the **Start Up Voltage** circuitry from powering VR2 and VR3.

VRAW2 generated by the power supply Output section powers VR2 and VR3. VR2 generates the stable +12 VDC output to J2, pin 4. VR3 generates the stable +12 VDC VREF2 that powers K1. VR4 receives -16 VDC from the power supply Output section and provides the stable -12 VDC output at J1, pin 2 and J2, pin 6.

Fault Monitor circuitry shuts down the power supply oscillator if the +5 VDC or VRAW2 voltages drop below acceptable standards. Circuitry consists of zener diodes CR19 and CR13, transistors Q10, Q8, Q7, and Q6, and associated circuitry.

The +5 VDC power supply output is input to the cathode of CR13 through resistor R44. As long as the +5 VDC power supply output is more than +4.7 VDC, Q8 is forward biased. When Q8 is on, Q7 is biased off and the voltage on U2, pin 6 remains high.

If the +5 VDC power supply output drops below +4.7 VDC, Q8 stops conducting and Q7 is forward biased. When Q7 conducts, a negative pulse is passed across capacitor C38 to U2, pin 6 and the Delay-Restart circuitry starts over. U2, pin 5 goes high, disabling the Oscillator output. VREF2 is removed and K1 de-energizes and starts the Start Up Voltages and degausses the CRT again.

If the VRAW2 drops to less than +12 VDC, CR19 is not reverse biased enough and Q10 is no longer forward biased. Q10 collector goes positive and puts a high voltage on U1, pin 10, and the base of transistor Q6. Pin 10 of U1 stops the Oscillator output, +5 VDC power supply output drops, and the Delay-Restart circuitry starts over again as described above. The positive voltage on the base of Q6 resets the Auto/Manual Degaussing circuits.

Current Limiting circuitry terminates the pulse width from the PWM oscillator when output current demands exceed the safe operating limit of the power supply. Circuitry consists of transformer T3, diode CR1, potentiometer R7, and associated circuitry.

The current flowing through the primary of T2 also flows through the primary of T3. Induced voltages to the secondary of T3 are rectified by diode CR1 and positive pulses are fed to the current sense input of U1, pin 4. Grounded pin 5 of U1, is biased by an internal bias supply to 200 mV above ground. When the current through the primary of T3 exceeds the value which delivers 200 mV or greater to pin 4 of U1, the internal comparator terminates the output of the PWM oscillator, protecting Q1 from excessive collector current.

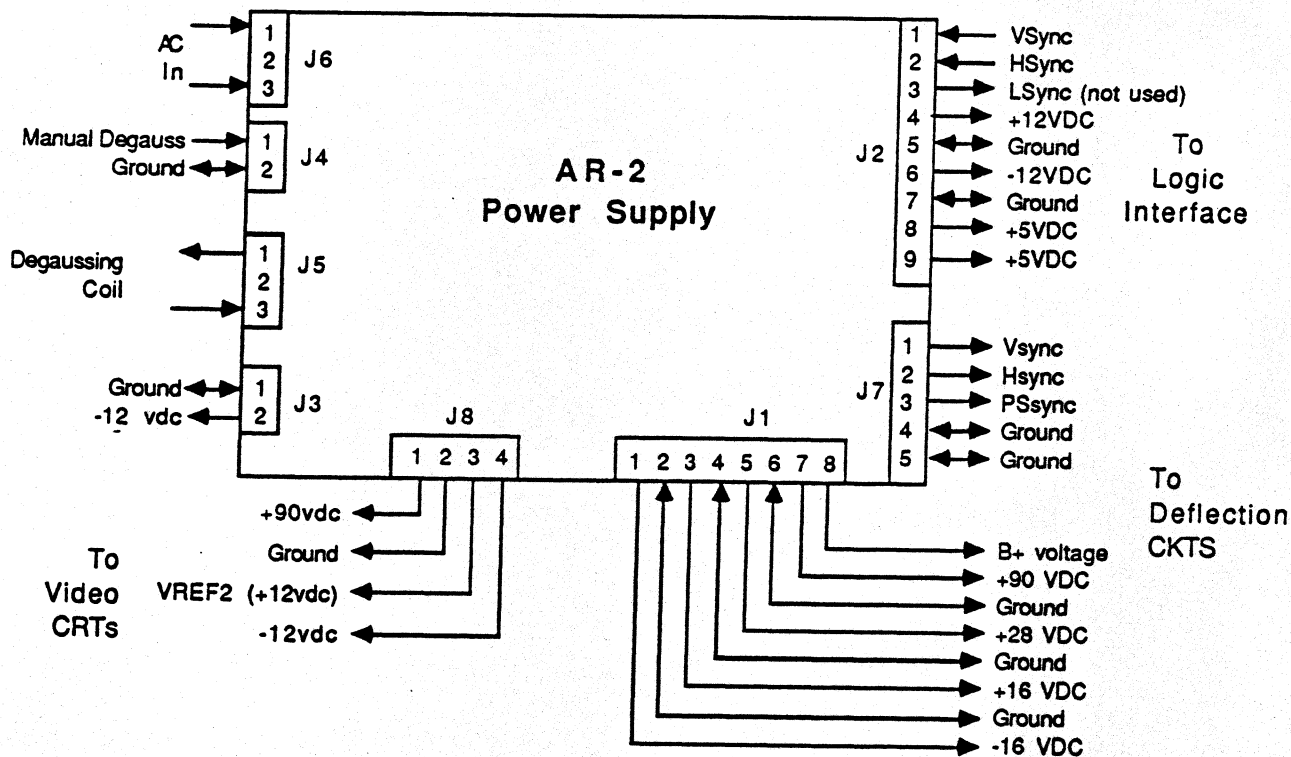
AR-2 POWER SUPPLY

Refer to schematic drawing #105682 rev 1 or later for the AR-2 power supply.

The AR-2 is Intecolor's second generation of "auto-ranging", switching, power supplies. It automatically adjusts for line voltage variations of 86 to 250 VAC, and line frequency variations of 40 to 70 Hz while maintaining stable output voltages. This allows the AR-2 power supply to be used anywhere in the world without requiring changes in jumpers or switches to accommodate different line voltages and frequencies.

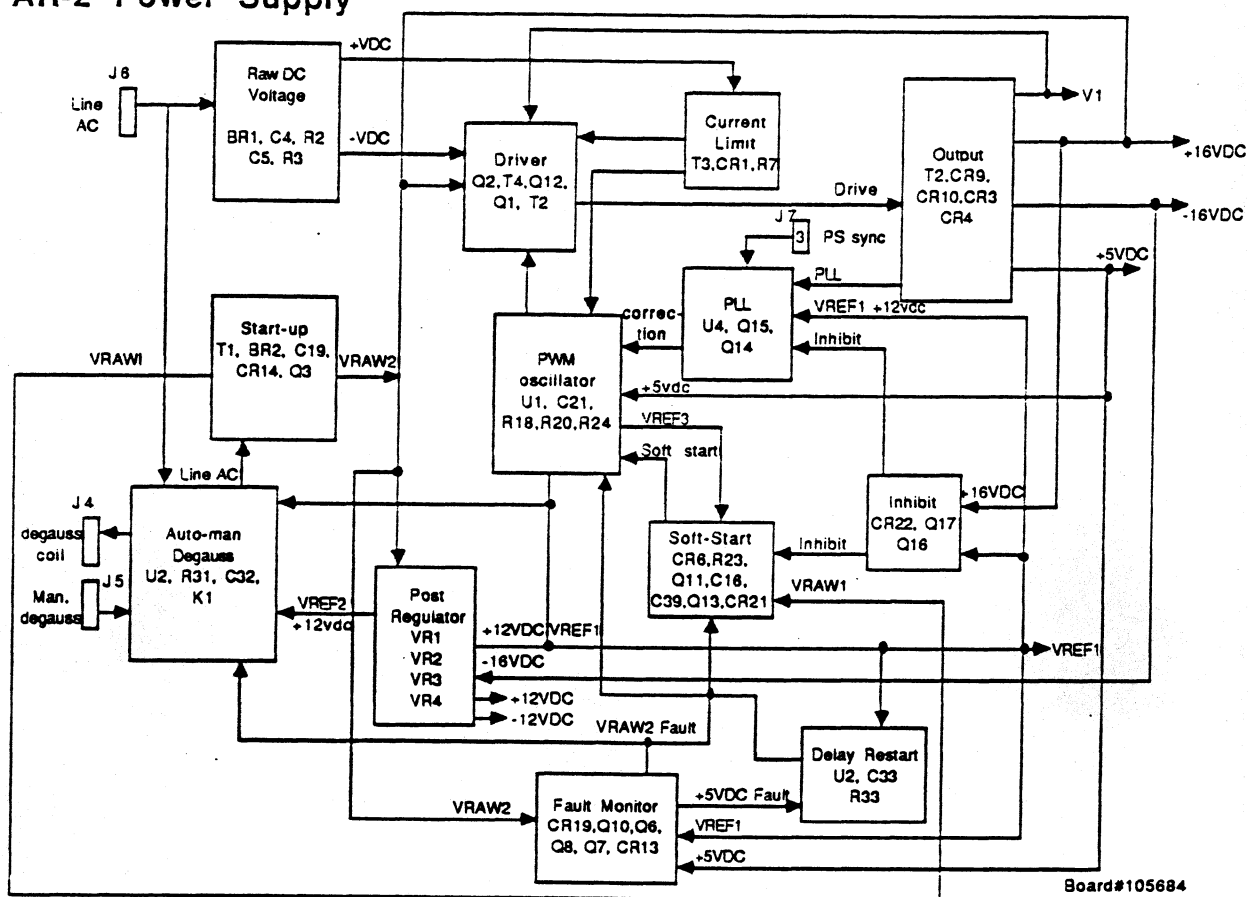
The AR-2's design is very similar to that of the KM-3 and KM-4 power supplies. Additional circuitry in the AR-2 power supply forms a Phase Locked Loop (PLL) for greater noise rejection in the output voltages.

Input and Output wiring



BLOCK DIAGRAM

AR-2 Power Supply



Board#105684
Schematic#105682

Circuit Description:

Start Up Voltage: This section contains a conventional linear type power supply with a specially designed transformer to operate over a broad range of line frequencies and voltages. The circuitry provides the switching regulator with an operating voltage for a short period of time when power is first applied to the unit or the Auto/Man Degauss circuit is activated. Components T1, BR2, C19, CR14, and others make this circuit work.

Line AC is input at J6, to the Raw DC Voltage circuits, and through relay K1 to the Start Up Voltage circuits. Current flows through normally closed contacts of relay K1 (pin 7 and 6), transformer T1, posistor RT2, and back to J6. The voltage is stepped down by T1 and then rectified into a DC voltage (VRAW1) by BR2 and filtered by capacitor C19. VRAW1 typically ranges from +12 VDC to +65 VDC determined by the line voltage.

VRAW1 is used by the Soft Start circuitry to detect the presence of high line voltage.

Transistor Q3, resistor R26, and 30 volt zener diode CR14, form a series-pass regulator to limit the output voltage (VRAW2), to +30 VDC. VRAW2, provided by T1, is an intermediate voltage supplied to the Post Regulator section and Switching circuits section during start up. VRAW2 is also an input to the Fault Monitor section.

Shortly after the power supply comes up to full operating potential, K1 opens the path for current to flow through T1. By this time, VRAW2 is provided by the power supply itself through diode CR8. Capacitor C30 provides a smooth transition from the T1 VRAW2 and the VRAW2 provided by the power supply.

Diode CR15 protects Q3 from damage when VRAW2 is provided by the power supply. CR8 prevents VRAW2, as provided by T1, from supplying the other regulators in the Post Regulator section.

Line voltages around 250 VAC will damage T1 if K1 fails to open at its pins 6 and 7. RT2 is a positive coefficient resistor that protects T1 when the line voltage is high and K1 fails. If line voltage is 250 VAC and K1 fails, current flow causes RT2 to heat up and open after about 30 seconds. RT2 should never activate under normal conditions. Should RT2 activate, five minutes cooling time should reset RT2.

Raw DC Voltage circuitry converts the AC line voltage into unregulated DC voltages for the Switching circuits main switching transistor and transformer. Circuitry consists of Y-capacitors C1, C2, and C6, X-capacitor C3, full wave bridge rectifier BR1, and associated components.

Line AC is input through J6 and rectified by full wave bridge BR1. The DC voltages are filtered by capacitors C4 and C5, while resistors R2 and R3 provide safety bleeder current. Positive DC output (across R3) provides current to the main switcher through F1. **WARNING:** The negative side of the output (Delta Ground) floats with respect to chassis ground. Use extreme caution when making measurements in this circuitry.

The special X and Y capacitors, C1, C2, C3, and C6, form part of an EMI/RFI filter. These capacitors must meet IEC standards, and should be replaced with the same approved type capacitors. Additional filtering, in the form of the line filter, is necessary to complete the EMI/RFI filtering to meet FCC requirements.

Negative coefficient thermistors installed in the AC input lines provide in-rush current protection. As these resistors heat up, their resistance decreases.

Delay-Restart circuitry delays the output of the Pulse Width Modulated Oscillator for 3 to 5 seconds and discharges the Soft Start capacitors. One half of U2, a 556 IC dual timer, and associated circuitry provide this function.

When VREF1 reaches approximately +5 VDC, U2 starts to operate. The time delay for this half of U2 is determined by resistor R33 and capacitor C33. U2, pin 5 is high approximately 3 to 5 seconds.

The high at U2, pin 5 is at U1, pin 10, and insures that U1 remains shut-down long enough for VREF1 to reach a stable +12 VDC output. The high from pin 5 also biases a transistor in the Soft Start circuitry on, which discharges the Soft Start capacitors and disables the pulse width modulated oscillator output.

When the Delay Restart circuits time out (3 to 5 seconds), U1, pin 10 goes low and the power supply begins providing the VRAW2 voltage to the Post Regulator section.

The Delay Restart circuitry can be forced to start over if the Fault Monitor circuitry detects a drop in the +5 VDC from the power supply output.

Auto/Manual Degaussing circuitry allows degaussing of the CRT and prevents K1 from interrupting current flow through T1 prematurely. Each time power is turned on or the manual degauss button is pressed, the screen of the CRT is degaussed. Circuitry consists of 1/2 of U2, relay K1, and associated circuitry.

When VREF1 reaches approximately +5 VDC, U2 starts to operate. The time delay for this half of U2 is determined by resistor R31 and capacitor C32. U2, pin 9 is high approximately 6 to 9 seconds. During this time, AC current flows through the contacts of relay K1 and a coil surrounding the face of the CRT.

The high from pin 9, of U2 biases transistor Q9 on. When Q9 conducts, Q5 is biased off and K1 cannot energize. While K1 is de-energized, current flows through T1 and the degaussing coil of the CRT. RT1 allows a large initial current flow through the degaussing coil. As RT1 heats up, it's resistance increases, thus gradually reducing the current flow through the degaussing coil to provide proper degaussing action.

Notice that the **Delay Restart** circuitry allows the power supply to start producing output voltages a few seconds before the current through T1 is interrupted. T1 generated VRAW2 is maintained briefly, allowing time for the power supply output voltages to stabilize.

The **Auto/Manual Degaussing** circuits can be forced to restart by the **Fault Monitor** circuits or a manual degauss input. The **Fault Monitor** or the manual degauss input will short pin 1 of J5 to ground. Capacitor C34 discharges and passes the low pulse to U2, pin 8. A low on pin 8 resets the **Auto/Manual Degaussing** side of U2. U2, pin 9 goes high and that side of the timer starts over again.

Diode CR12, across the coil of K1, protects Q5 from the kick-back voltage generated by the collapsing field around the core of K1 when Q5 turns off.

Soft Start circuitry prevents the power supply from destroying itself by starting too quickly. Circuitry consists of diode CR6, transistors Q11 and Q13, and associated circuitry.

When line voltage is larger than 180 VAC, a VRAW1 greater than +39 VDC is generated by BR2. Zener diode CR18 is sufficiently reversed biased to bias Q13 on and C39 is in the circuit.

The high provided by U2, pin 5, is on the base of Q11, biasing it on. Q11 discharges capacitor C16 (and C39 when line voltage is large enough) and forward biases CR6 to hold down pin 9 of U1. When Q11 is biased off, by U2, pin 5 going low, C16 (and C39) charge toward VREF3 (+5 VDC) provided by U1, pin 16, through resistor R23. C16 (and C39) charging toward +5 VDC gradually decrease forward bias on CR6 and allows U1, pin 9 voltage to rise. U1 contains a pulse width modulator (PWM) circuit. The voltage on pin 9 controls the width of the PWM output pulses; lower voltage results in narrower pulses. By forcing pin 9 low and allowing its voltage to rise slowly, power supply soft start is made certain.

Oscillator circuitry provides the **Switching** circuitry with a regulated pulse width modulated square-wave. Circuitry consists of U1, capacitor C21, potentiometer R24 and associated components.

U1 is a special voltage controlled, pulse width modulated, oscillator IC. Capacitor C21 on pin 7, and resistor R18 on pin 6, provide an RC network for the oscillator in U1. When VREF1 is input to U1, pin 15 a ramp signal is developed at pin 7. VREF3 is generated by U1 and is a highly stable +5 VDC output at pin 16.

The +5 VDC power supply output is used as feedback through resistor R57, adjusted by R24, and input to U1, pin 1. VREF3 is used as a reference voltage through resistor R20 and input to U1, pin 2. The voltage on U1, pin 1 is adjusted to set the +5 VDC power supply output.

Power supply regulation is as follows:

An internal error amplifier compares voltages on U1, pins 1 and 2, and outputs an error signal that can be observed at pin 9. This error voltage can be over-ridden by either the Current Limiting circuitry input at pin 4, or Soft Start circuitry connected to pin 9.

If the +5 VDC power supply output voltage tries to increase, such as when current demands decrease. The feedback voltage to U1, pin 1 rises higher than pin 2, and the error voltage at pin 9 decreases.

When the ramp signal at U1, pin 7, exceeds the error voltage at pin 9, the output of the PWM comparator is disabled. The width of positive pulses output from U1, pin 11 are decreased and the power supply reduces its output.

If the +5 VDC power supply output voltage tries to decrease, such as when current demands increase. The feedback voltage to U1, pin 1 drops lower than pin 2, and the error voltage at pin 9 increases.

When the error voltage exceeds the ramp voltage, the output of the PWM comparator is enabled. The width of positive pulses output from U1, pin 11 are increased and the power supply output voltages increase. A high at U1, pin 10 disables the output of the PWM.

Phase locked loop and Power Supply Sync circuitry phase locks and synchronizes the power supply with the deflection board horizontal drive frequency. Circuitry consists of U4, transistors Q15, Q14, and associated circuitry.

"PS SYNC", derived from HSYNC in the deflection board, is inverted by transistor Q14 and provides one input to PLL IC U4, pin 14. A pulse from transformer T2, pin 8 (power supply output) provides another input for the phase comparator U4, pin 3. Transistor Q15 and diode CR7 invert the pulse and insures that it is a square wave shape.

The phase detector portion of U4, generates a pulse train at U4, pin 13. Resistor R10 and capacitor C43 integrate the pulses into a DC voltage, input at U4, pin 9, proportional to the PS SYNC and the switching power supply's turn-off time. This voltage is buffered by U4 and output at pin 10 to the oscillator U1, pin 7.

The voltage at U4, pin 10, increases or decreases the rate of charge of the ramp capacitor for U1, pulse width modulator, C21. By modulating the rate of charge for C21, in response to the phase difference between the PS SYNC and the power supply output, the oscillator is maintained in phase with the deflection board horizontal drive frequency.

Inhibit circuitry, inputs a TTL high at U4, pin 5. When this pin is high, the output, pin 10, is low.

Inhibit circuitry dissables the Phase Locked Loop circuitry long enough for the power supply outputs to stabilize. This circuitry also prevents the power supply from restarting when high line voltage is present and a manual degauss cycle is activated. Circuitry consists of zener diode CR22, transistors Q17 and Q16, and associated components.

Q17 collector is tied to U4, pin 5 and VREF1 through resistor R72. The Phase Locked Loop output is inhibited when Q17 is biased off. Q17 is biased on by the +16 VDC power supply output reverse biasing 12 volt zener diode CR22.

A manual degauss input with high line voltage (CR18 passes voltage) can bias Q13 on. In this situation, pin 9 of U1 could be low long enough for the power supply to shut itself down. Inhibit circuitry removes the base bias of Q13 to prevent this from happening.

Once the +16 VDC output is present, CR22 passes voltage and transistor Q16 is biased on. Q16 conducts, removing the bias voltage from the base of Q13.

Switching circuitry provides a controlled AC voltage for the power supply Output section. Circuitry consists of transistors Q2, Q12 and Q1, transformers T4 and T2, and associated components.

The Oscillator output is at the base of Q2. During initial start-up of the switching circuitry, VRAW2 (generated by T1) provides supply voltage for T4 and Q2. Once the power supply provides output voltages, +90VDC is the primary source voltage for T4 and Q2. Diode CR16 prevents +90VDC voltage from entering VRAW2 while diode CR2 prevents VRAW2 from powering +90VDC circuits.

Positive pulses bias Q2 on, current flows into pin 1 of T4 and a positive voltage is applied to T4, pin 6. Transistor Q1 is biased on and current flows from Delta Ground through Q2 and the primary of T2. A positive voltage is applied to pin 1 of T2. Polarity dots drawn on the schematic show that the secondary output diodes are reverse biased and no energy is transferred to the secondaries. Energy is stored in the core of T2 in the form of a magnetic field.

When Q2 is switched off by the oscillator output, Q1 is biased off. The collapsing field induces a voltage in the secondary windings which forward biases the secondary diodes and energy is drained from T2 into the output capacitors.

In a switching circuit where a transistor is required to turn-off an inductive load, the collector is subjected to current and voltage stresses at the same time. Capacitor C7, resistors R4 and R16, and diode CR5 form a turn-off "snubber" to protect Q1 from induced stress. As Q1 turns off, the T1 primary inductor current begins to flow through C7 and CR5, charging C7. Once the inductor current subsides, R4 and R16 discharge C7 so that the "snubber" is ready for the next cycle of the switching circuitry.

Besides snubbing the turn-off current away from Q1, it is also necessary to turn Q1 off quickly to minimize the peak power dissipated.

When Q2 is biased on, positive current flows into the base of Q1, out the emitter and back to pin 5 of T4 through resistor R61, capacitor C10 and diode CR20. This positive current turns Q1 on and charges C10 to a value determined by R61.

When Q2 is biased off, transistor Q12 is biased on, placing C10 between the base and emitter of Q1. The charge on C10 reverse biases Q1 base to emitter and ensures that it turns off quickly.

Resistor R12 aids in turning off Q1 while capacitor C17 helps turn Q12 on quickly.

Diode CR17 and resistor R11 control the shape of the turn-off pulse delivered to the base of Q1.

NOTE:

The schematic shows that Q1 transistor may be either a BUX88 or MJ8505. The MJ8505 transistor is preferred for reliable long term circuit operation. The BUX88 transistor will run typically 10 degrees hotter than the MJ8505, which impacts long-term reliability.

Intecolor checks the Beta of all the transistors installed as Q1. Transistors with Beta less than 18 are preferred, but some power supplies have been modified to accept Q1 transistors with Beta up to 25. The modification is in the Base Drive circuitry; resistor R49 may be changed from a 56 ohm to a 120 ohm resistor.

Output circuitry rectifies and filters the AC voltage provided by the **Switching** circuits to generate the output voltages. Circuitry consists of, the secondaries of T2, diodes CR21, CR9, CR10, CR3 and CR4, and associated components.

CR21 allows positive pulses to develop a +28 VDC charge across capacitor C44, output at J1, pin 5. Resistor R60 provides a nominal load for the +28 VDC output, should the output loads be removed.

CR9 allows positive pulses to charge C9 and produce the VRAW2 voltage and +16 VDC output at J1, pin 3.

CR10 allows negative pulses to charge C11 and produce the -16 VDC output to the **Post Regulator** section and J1, pin 1.

CR3 is a paralleled Schottky diode pair. CR3 allows positive pulses to capacitors C10 and C48 to charge and produce the +5 VDC that is used as feedback for regulation, monitored by the **Fault Detect** circuits and is output to J2, pin 8,9. Since the +5 VDC is used for regulation, R28 provides a minimal load if the external load is removed.

CR4 allows positive pulses to charge capacitor C12 and produce the high V1 voltage (+70 to +90 VDC) that is output to J1, pin 7, and the **Switching** circuit. Since the +90VDC is used as a supply voltage for a transistor in the **Switching** circuits, resistor R29 provides a minimal load if the external load is removed. Jumper W2 allows a selection of two different +90VDC values.

Optional circuitry (diode CR23 and associated components) would generate a B+ DC voltage for deflection boards that require it. For 8800 series terminals this circuitry is not installed and jumper W1 is in place.

Post Regulator circuitry generates regulated low voltage outputs for various circuits on the board and provides +12 VDC and -12 VDC outputs to the output connectors on the board. This circuitry consists of regulators VR1, VR2, VR3, and VR4 with associated components.

VRAW2 provided by the **Start Up Voltage** circuitry or the power supply **Output** section provides supply voltage for VR1. VR1 generates the stable +12 VDC VREF1.

Diode CR8 prevents the VRAW2 generated by the Start Up Voltage circuitry from powering VR2 and VR3.

VRAW2 (+16 VDC) generated by the power supply Output section powers VR2, VR3 and VR1 once the T1 generated VRAW2 is removed. VR2 generates the stable +12 VDC output to J2, pin 4. VR3 generates the stable +12 VDC VREF2 that powers K1 and is output at J8, pin 3.

VR4 receives -16 VDC from the power supply Output section and provides the stable -12 VDC output at J2, pin 6 and J8, pin 4.

Fault Monitor circuitry shuts down the power supply oscillator if the +5 VDC or VRAW2 voltages drop below acceptable standards. Circuitry consists of zener diodes CR19, and CR13, transistors Q10, Q8, Q7, and Q6, and associated circuitry.

The +5 VDC power supply output is input to the cathode of CR13 through resistor R44. As long as the +5 VDC power supply output is more than +4.7 VDC, Q8 is forward biased. When Q8 is on, Q7 is biased off and the voltage on U2, pin 6 remains high.

If the +5 VDC power supply output drops below +4.7 VDC, Q8 stops conducting and Q7 is forward biased. When Q7 conducts a negative pulse is felt across capacitor C38 to U2, pin 6 and the Delay-Restart circuitry starts over. U2, pin 5 goes high, disabling the Oscillator output. VREF2 is removed and K1 de-energizes and starts the Start Up Voltages and degausses the CRT again.

If the VRAW2 drops to less than +12 VDC, CR19 is not reverse biased enough and Q10 is no longer forward biased. Q10 collector goes positive and puts a high voltage on U1, pin 10, and the base of transistor Q6. Pin 10 of U1 stops the Oscillator output, +5 VDC power supply output drops, and the Delay-Restart circuitry starts over again as described above. The positive voltage on the base of Q6 resets the Auto-Man Degauss circuits.

Current Limiting circuitry terminates the pulse width from the PWM oscillator when output current demands exceed the safe operating limit of the power supply. Circuitry consists of transformer T3, potentiometer R7, and associated circuitry.

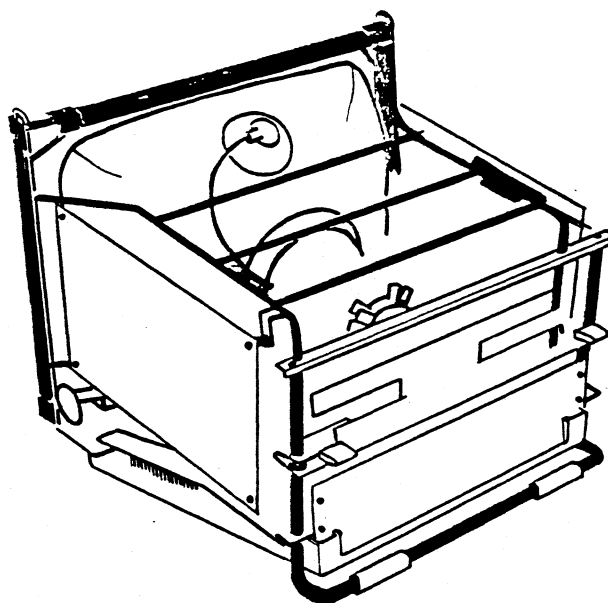
The current flowing through the primary of T2 also flows through the primary of T3. Induced voltages to the secondary of T3 are rectified by diode CR1 and positive pulses are fed to the current sense input of U1, pin 4.

Grounded pin 5 of U1, is biased by an internal bias supply to 200 mV above ground. When the current through the primary of T3 exceeds the value which delivers 200 mV or greater to pin 4 of U1, the internal comparator terminates the output of the PWM oscillator, protecting Q1 from excessive collector current.

THE DEFLECTION BOARD

The Deflection assembly generates the high CRT anode voltage, screen grid voltage, focus grid voltage, and control grid voltage. Linear deflection currents to drive the horizontal and vertical deflection coils in the CRT yoke are also provided by the deflection circuitry.

The deflection board is located on the left side when looking at the rear of the monitor.



Identification of the Deflection boards and relative schematics is shown below.

		Schematic	Board
3800	KM-3 Deflection	# 103300	# 103302
3800	KM-4 Deflection	# 105761	# 105763
8800	AR-2 Deflection	# 105155	# 105157

KM-3 and KM-4 DEFLECTION

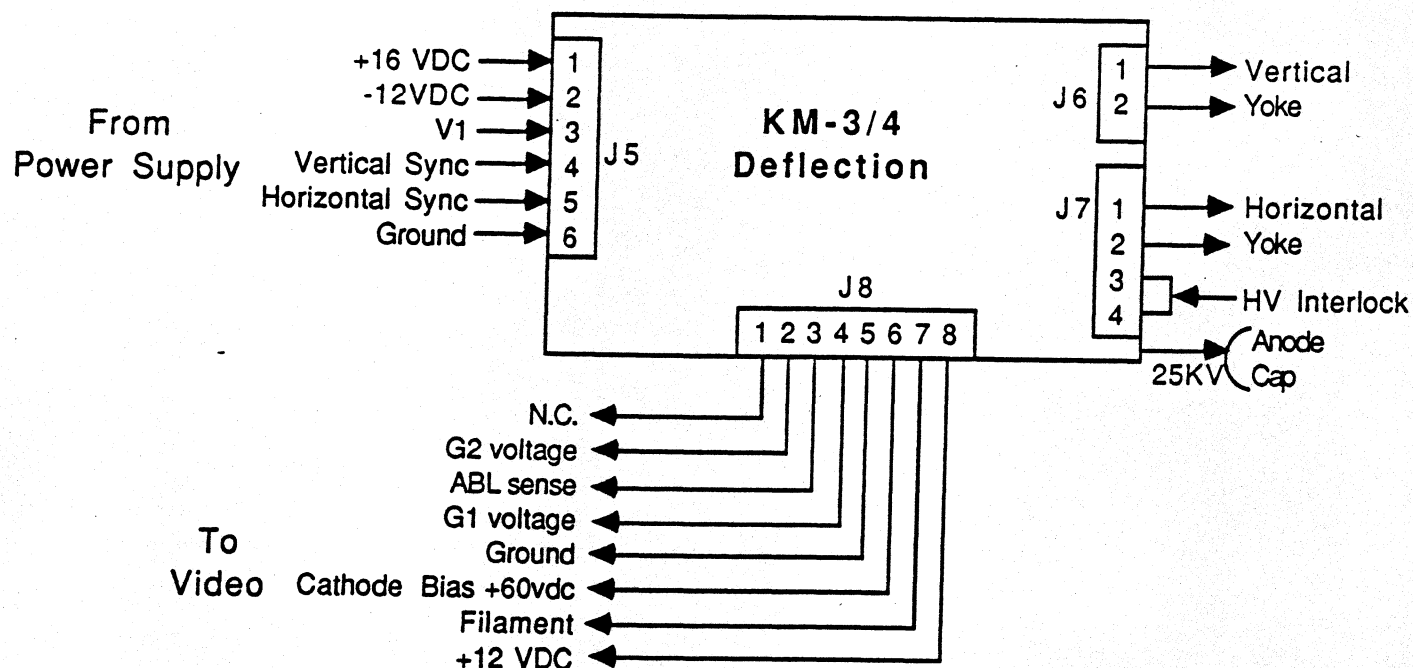
Refer to schematic #103300 Rev 1 or later for the KM-3 deflection board.

Refer to schematic #105751 rev 1 or later for the KM-4 deflection board.

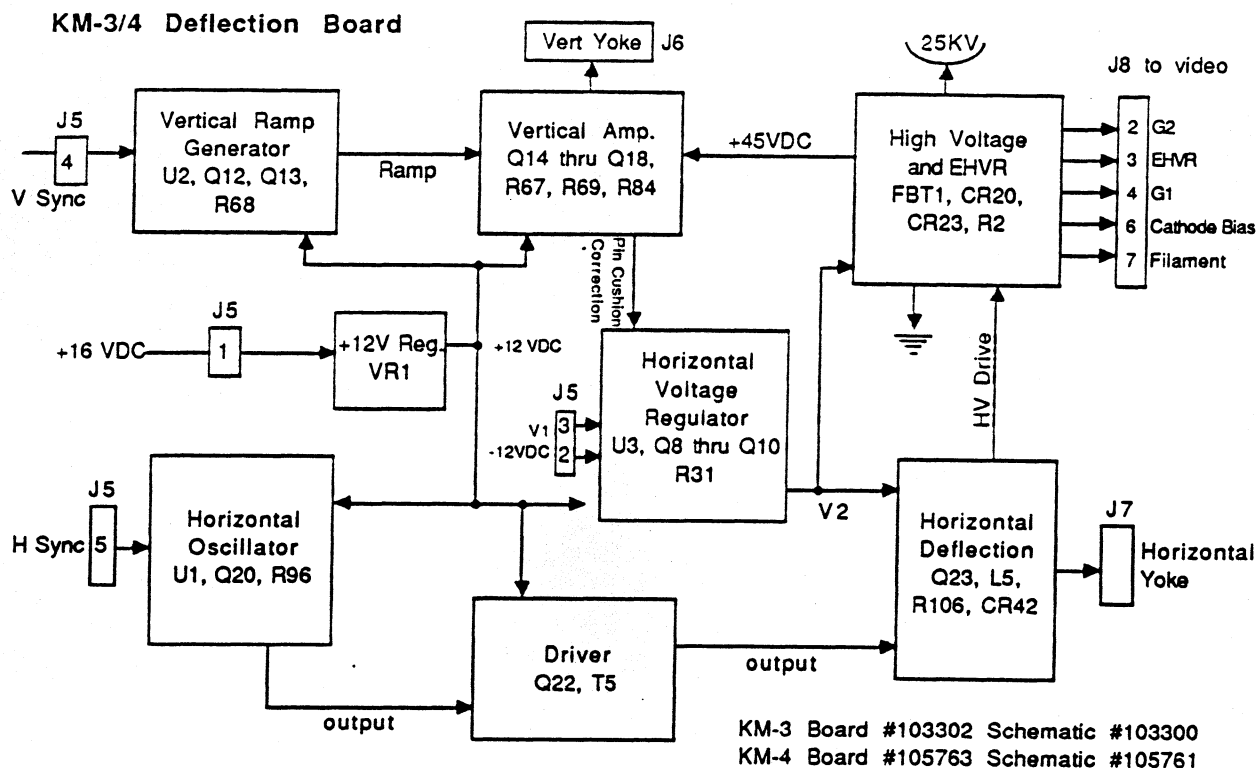
The KM-4 and the KM-3 deflection boards are almost identical electronically. The KM-4 board is the latest revision of the KM-3 board. Connector J9, an optional brightness control on the KM-3, was omitted on the KM-4 board. This option is no longer used. These deflection boards are used in many Intecolor 14" terminal products.

Circuitry on the board generates the 25 KV anode voltage, synchronized deflection yoke drive signals, CRT heater voltage, +60 VDC cathode bias voltage, and control grid (G1) voltage. The flyback transformer is mounted to the deflection board and allows focus control and screen grid (G2) bias control.

Input and Output Wiring



BLOCK DIAGRAM



Circuit Description:

Vertical Ramp Generator circuitry provides a linear voltage sawtooth, synchronized with the logic board, for the vertical amplifier. Circuitry consists of U2, transistors Q12, Q13 and associated circuitry.

A sawtooth waveform is generated by an NE555 timer, U2, and its associated components. U2 is configured as an astable multivibrator that can free-run but will restart itself when an external sync trigger is applied.

An external sync trigger is input to U2, pin 4, through level-shifting transistor Q12, to synchronize the vertical deflection with the video from the logic.

The output at pin 6 is a voltage ramp rising from ground toward +12 VDC, developed by charging capacitors C42 and C43 in series with resistors R63 and R64. When pin 6 reaches 2/3 of the (+12 VDC) supply voltage, or when the trigger input pin 4, goes high, pin 7 switches low and discharges C42 and C43 through R64. Since R63 and R64 together provide a long charge time and R63 through pin 7 to ground provides a short discharge time, the output at pin 6 is a sawtooth with slow rise and fast fall times.

The sync trigger from the logic limits the rise of the sawtooth and cuts short the length of the sawtooth. When no sync trigger is present the multivibrator will free-run with a slightly longer rise time on the sawtooth.

Feedback for the ramp generator is from the emitter of amplifying transistor Q13 through potentiometer R68 and resistor R65 to the connecting point between C42 and C43. R68 is adjusted for a linear current ramp through the vertical deflection coil.

Vertical Amplifier circuitry produces a linear current ramp through the vertical deflection yoke using the vertical ramp generator output and generates a parabola shaped signal at the vertical rate to correct for vertical pincushion effects. Circuitry consists of potentiometer R67, transistors Q14 through Q17 and associated circuitry.

With no current flowing through the vertical deflection coils, the beams from the CRT cathodes would strike the CRT at the center of the screen. The deflection coils, when current flows through them, function like an electromagnet, deflecting the beams to the top or bottom of the screen. The direction of current flow determines which direction the beams are deflected, while the amount of current determines how far the beams are deflected. The rate of change of the current flow controls the velocity of the movement. Current flow of a constant value would deflect the beams to the top or bottom of the screen and hold them there until the current flow changes direction or value.

With this information in mind, it can be determined that an alternating current (that which changes direction and value) would repeatedly drive the beams from the center to the top or bottom of the screen, back through the center to the other end of the screen.

Current flow for vertical ramp generator amplifier Q13 is from ground through resistors R81, and R69, potentiometer R67, and resistor R66. By controlling the input, vertical size potentiometer R67 is used to set vertical output level.

Capacitor C44 couples the ramp signal to transistor Q14 and provides DC isolation to allow the DC operating point of Q14 to be set by feedback through resistors R71 and R72. Q14 inverts the signal and controls the push-pull transistor network of Q15, Q16 and Q17.

When the electron beam is at the top of the screen, the ramp output from the ramp generator is starting from its lowest potential. Q14, Q15 and Q17 are biased for minimum conduction. Q16 is biased for maximum conduction. Current flow through the yoke is maximum.

Current flows from ground through R81, capacitor C49, out pin 2 of J6, through the vertical yoke, back in pin 1 of J6, through diode CR32, resistor R79 and Q16 to the +45 VDC supply. Capacitor C49 develops a DC average voltage (about half of the +45 VDC), set by transistor Q19 and potentiometer R69. This is used as feedback, through resistor R71, to set the vertical center.

As the ramp progresses, Q14, Q15 and Q17 begin to conduct more, while Q16 begins to conduct less. Current flow through the yoke decreases because Q17 provides another path for current to flow from ground to the +45 VDC. As current decreases through the yoke, the beam moves toward the center of the screen.

When the beam is at the center of the screen, the ramp from the ramp generator is at its midpoint, Q17 and Q16 conduct equally and no current flows through the yoke.

Because of the base to emitter voltage drop of about .6VDC for Q15 and Q16. Q16 and Q17 will not reach equalization at the same time. Diodes CR30 and CR31 establish stable bias on Q16 and Q15 by compensating for the base to emitter voltage drop of these two transistors. The temperature coefficients of the diodes complement the coefficients of the transistors to improve temperature stability.

As the ramp progresses, Q17 conducts more and Q16 conducts less. Current begins to flow through the yoke in the opposite direction: from ground, through Q17 to the parallel path of Q16 to the +45 VDC and through the deflection yoke to the positive charge on C49. As Q16 decreases conduction, current through the yoke increases and the beam moves toward the bottom of the screen.

When the beam is at the bottom of the screen, current through the yoke is maximum and the ramp is ending. Q16 is at minimum conduction and Q17 is at maximum conduction.

When the ramp ends and goes negative quickly, Q14, Q15, and Q17 turn off. Current through the yoke decreases and the beam starts to retrace to the middle of the screen.

Capacitor C46 provides feedback to insure that Q16 comes up to maximum conduction quickly. Current through the yoke reverses direction and completes the retrace to the top of the screen. When current through the yoke decreases to minimum and then increases to maximum a large positive voltage spike is developed. Diode CR32 provides protection for Q16 while capacitors C47 and C48 help limit the size of the pulse.

A parabolic voltage waveform developed across C49 is amplified by Q18 and used as a pincushion correction signal. This signal is applied to the input of the **Horizontal Deflection Voltage Regulator** in order to modulate the width of the horizontal beam trace. Potentiometer R84 can be adjusted for the appropriate size signal to make the sides of a full screen raster appear straight.

Horizontal deflection voltage regulator circuitry provides pincushion corrected, regulated DC voltage for the **Horizontal Deflection** circuitry and the **High Voltage** circuitry. The voltage regulator consists of operational amplifier U3, transistors Q10, Q9, Q8 and associated components.

Input of U3, pin 2 is connected to a voltage divider network between the +DC output voltage of Q8 and -12 VDC at R32 to permit adjustment of the reference voltage above and below ground. The parabolic wave signal from Q18 is combined with the reference voltage set by potentiometer R31 and input to U3, pin 2.

DC Feedback for the regulator is through the resistor selected by jumper W5 to potentiometer R31 and resistor R33 to U3, pin 2. If the output voltage goes high, the voltage on inverting pin 2 goes high. When that occurs, U3 output pin 6 goes low and Q10 collector goes high, biasing Q9 to conduct less. This decreases the bias voltage on the base of Q8. The output voltage of the regulator goes down until the voltage at U3, pin 2 is brought to zero. The parabola signal is input on U3, pin 2 with the feedback but is not cancelled by the effects of feedback. AC feedback, through capacitor C77, is for stability.

R31 adjusts the high voltage output (25 KV) at the CRT anode. The output voltage is developed on capacitor C87 and is called V2.

Horizontal oscillator circuitry provides a square wave signal synchronized with the horizontal sync from the logic. The oscillator circuitry consists of a phase-locked-loop voltage controlled oscillator U1, transistor Q20, potentiometer R96 and associated circuitry.

The free-running frequency of the voltage-controlled oscillator (VCO) in U1 is determined by the capacitance across pins 6 and 7 and the resistance across pins 11 and 12. The resistance between pin 12 and ground is adjusted to set the free-running frequency near the desired value.

The actual VCO frequency is controlled by a voltage input at pin 9. This control voltage is the output of a phase comparator within U1 which compares the HSYNC input (at pin 14, via Q20) with a sample of the CRT horizontal retrace pulse (at pin 3). The comparator develops a control voltage to keep the two inputs in phase, synchronizing the horizontal scan with the video signals from the logic board. The RC filters at pins 9 and 13 smooth the output of the phase comparator into a DC average.

The output of the VCO of U1, pin 4 is a 50% duty cycle square wave signal.

Driver circuitry amplifies the output of the **Horizontal Oscillator** and drives the **High Voltage** and **Horizontal Deflection** circuits. Transistor Q22, transformer T5 and associated circuitry provide this function.

Q22 driven by the **Horizontal Oscillator** drives the primary of T5. Resistor R103 limits current while resistor R105 and capacitor C66 limit ringing in primary of T5.

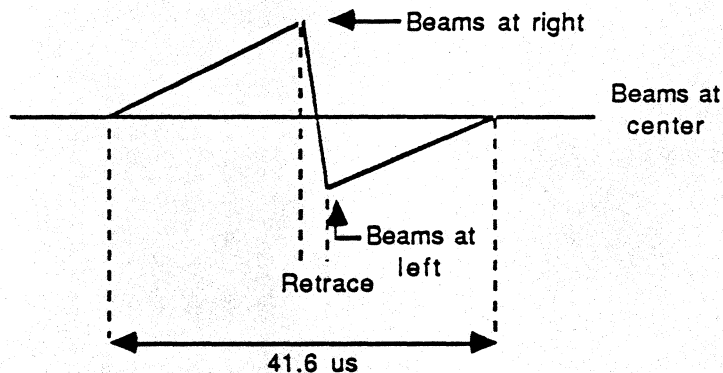
Horizontal deflection circuitry provides a current ramp with slow linear rise and fast fall time for the horizontal deflection yoke. The horizontal deflection circuitry also provides switching for the flyback to develop the high voltage at the CRT anode. Circuitry consists of transistor Q23, diode CR42, variable inductor L5, and transformer T7 and associated circuits.

With no current flowing through the horizontal deflection coils, the beams from the CRT cathodes would strike the CRT at the center of the screen. The deflection coils, when current flows through them, function like an an electromagnet, deflecting the beams to either side of the screen. The direction of current flow determines to which side of the screen the beams are deflected, while the amount of current determines how far the the beams are deflected. The rate of change of the current flow controls the velocity of the movement. Current flow of a constant value would deflect the beams to either side of the screen and hold them there until the current flow changes direction or value.

With this information in mind, it can be determined that an alternating current (that which changes direction and value) would drive the beams from the center to either side of the screen, back to center and then to the other side of the screen.

The alternating current, in an KM-3/4 deflection assembly, has a cycle time of about 41.6 microseconds, corresponding to a sweep rate of 24 kHz. At the beginning of a cycle, the current starts increasing linearly from zero to its peak value. As it does so, the beams are deflected from the center of the screen to the right side at a constant velocity. The current then changes direction very quickly, going from its peak positive value to its peak negative value in about 4.5 microseconds. The beams are deflected to the left side of the screen very quickly. This is called the "retrace" scan. At this point, the current through the yoke begins decreasing linearly from its peak negative value back to zero, and the beams are deflected to the center of the screen again. The process continues, with current changing directions and linearly increasing to its peak positive value.

It can be seen that the deflection coil current has a relatively slow linear sawtooth or ramp waveform with a very quick transition from peak positive value to peak negative value.



Transistor Q23 is switched on by the Driver circuits for a period slightly less than one half cycle of the horizontal frequency. Just before Q23 is turned on, current flow through the horizontal yoke is minimum and the beams are at the center of the screen. When Q23 is turned on, its emitter is raised to a potential about equal to the supply voltage (+60V). This voltage appears across the primary of the flyback transformer, FBT1, and current begins to flow in the primary winding. This current increases as energy is absorbed from the supply and stored in the transformers core.

At the same time capacitor C9, (selected by jumper W4A for 24kHz operation) begins to discharge through the inductive network which includes the horizontal deflection coil. (C9 was charged by a previous cycle.) Because of the resonant characteristics of the deflection circuit, C9 charges and discharges at a linear rate. Current through the coil increases at a linear rate to its peak positive value and the beams are deflected at a constant speed to the right side of the screen.

When Q23 is turned off, FBT1's primary current decreases abruptly, and a large voltage is induced on the primary which has a polarity opposite that of the DC supply. At this point CR42 is reverse biased and capacitors C84 and C80 (selected by jumper W9), are quickly charged by the inductive kick. When C84 and C80 are fully charged, the current through the deflection coil rapidly decreases to zero and the beams quickly go to the center of the screen. Because of the resonant characteristics of the deflection circuit, C84 and C80, charge and discharge very rapidly. When C84 and C80 discharge, the current through the deflection coil changes direction to its peak negative value and the beams are deflected to the left side of the screen (retrace). Diode CR42 protects Q23 from the large inductive kick (retrace pulse) produced when current reverses direction through the inductive components and prevents C84 and C80 from charging to the opposite polarity.

Current begins flowing through the deflection coil at a linear rate again as C9 begins to charge. The beams are deflected at a constant rate from the left side of the screen to the center.

The contour of the linear current ramp can be fine-tuned by inductor L4 to linearize the horizontal scan. L5 is adjusted to set the width of the horizontal deflection.

A bridge rectifier circuit associated with T7 produces a biasing current which is used to center the horizontal sweep on the screen. During the "on" time of Q23, voltage is induced in the T7 winding, and capacitors C71 and C70 are charged through diodes CR44 and CR43. Adjustment of potentiometer R106 varies the bias on pin 1 of the horizontal yoke, resulting in a displacement of the horizontal scan to the left or right on the screen.

High voltage and ABL circuitry produces the 25 KV desired at the CRT anode and develops a voltage to be used by the video board to provide Automatic Beam Current Limiting (ABL). Circuitry consists of FBT1, diodes CR20, CR1, CR23 and associated circuits.

The turning on of transistor Q23 completes a current path through the primary of flyback transformer FBT1 to ground. The flyback pulse which appears when Q23 is turned off is stepped up to the nominal 25 kilovolts through four secondary windings connected in series by steering diodes. This provides the desired output voltage at the anode of the CRT and is divided down to provide adjustable bias voltages for the focus grid and the G2 (screen) grid.

A portion of FBT1's primary current is rectified and filtered by diode CR23 and capacitor C32 to provide the +45 VDC required by the Vertical Deflection Circuitry. Diode CR20 and capacitor C30 produce a negative bias voltage from the same primary section for the G1 (CRT control grid) voltage. This voltage is regulated by 100 volt zener diode CR22. A third rectifier-capacitor combination, CR1 and C2, provides +60 VDC for the video driver assembly, output at J8, pin 6.

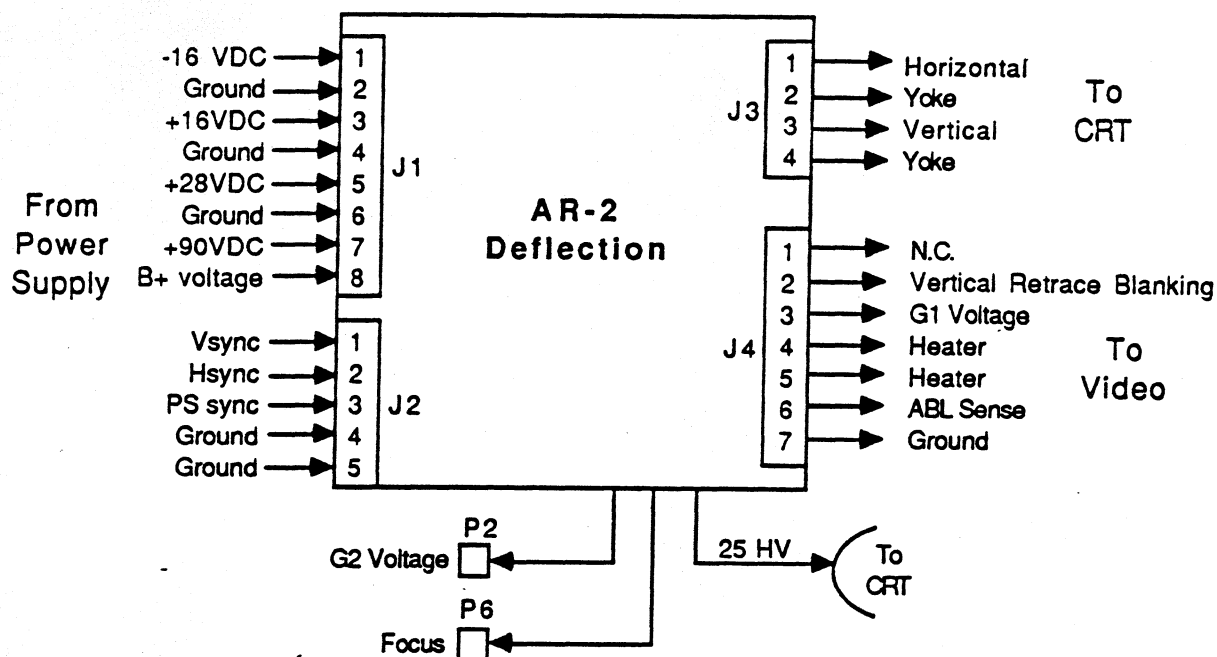
The filament voltage for the CRT heater is taken from another winding of FBT1. The AC voltage is output to the video board at J8, pin 7.

The FBT1 secondary tap at pin 5 is returned to ground through an AC-bypassed variable resistance which provides an adjustable voltage reference developed by capacitor C1. This voltage represents the amount of current flowing through the flyback at any given time. The voltage is output to the video board at J8, pin 3 to control the output of the video drivers. Beam current limiting provided by this circuit has the advantage of allowing the CRT to conduct larger currents under partial load conditions than would be possible otherwise.

AR-2 DEFLECTION

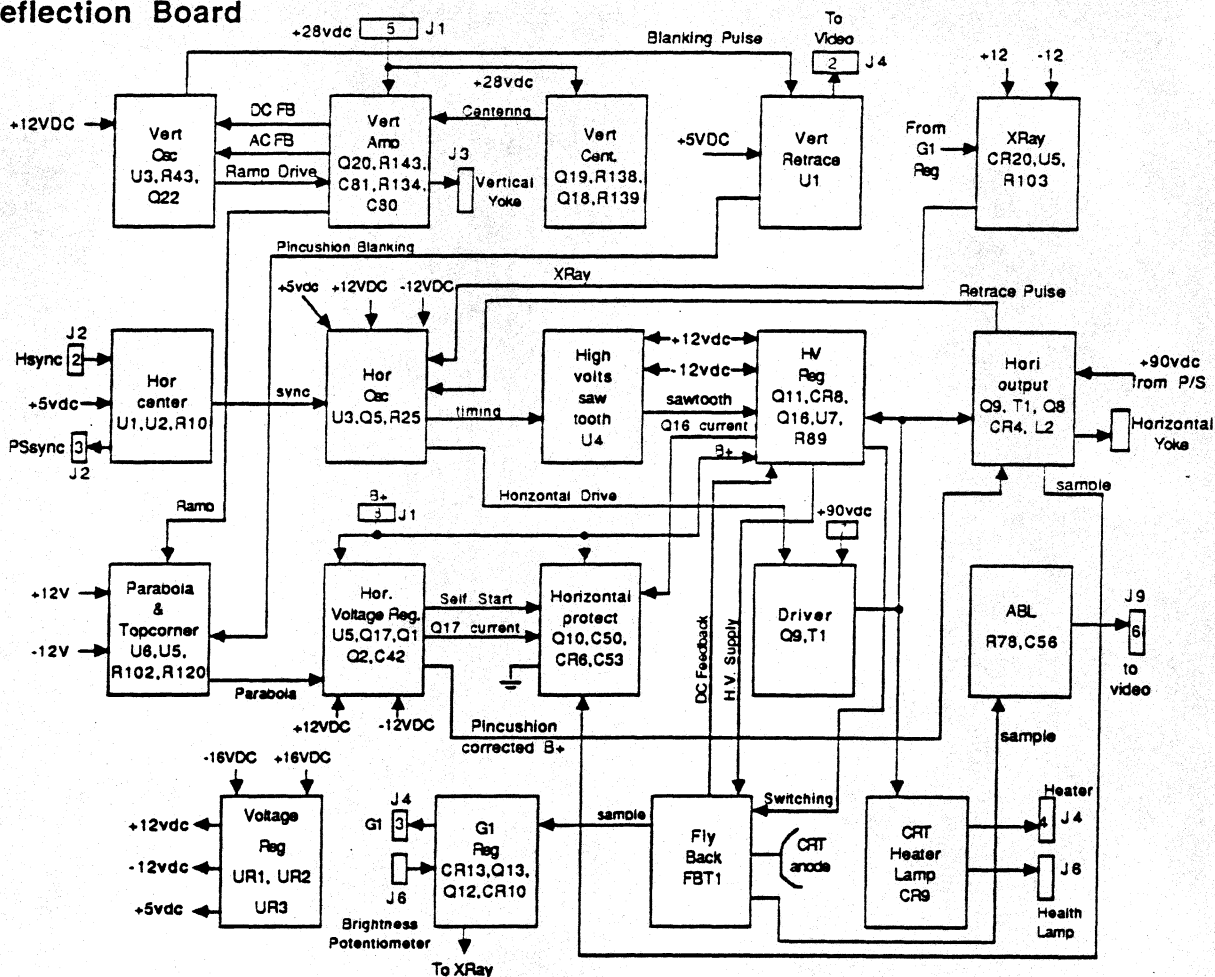
Refer to schematic #105155 REV 1 or later and the block diagram for the AR-2 deflection board.

The AR-2 deflection board is used in many Intecolor 19" CRT products. Circuitry on the board is responsible for generating the 25 KV anode voltage, synchronized deflection yoke drive signals, CRT heater voltage and CRT control grid bias voltage. The flyback transformer is mounted to the deflection board and allows focus control and G2 (screen) bias control.

Input and Output Wiring

BLOCK DIAGRAM

AR-2 Deflection Board



AR-2 Board # 105157
AR-2 Schematic # 105155

Circuit Description:

Vertical oscillator circuitry generates a vertical drive signal synchronized with the **VS**SYNC from the logic board and triggers the **Vertical Retrace Blanking** circuitry. Circuitry consists of 1/2 of U3, transistor Q22, potentiometer R43 and associated components.

A low true vertical sync signal from the power supply at J2 pin 1 is inverted by Q22 then input to U3, pin 1. Potentiometer R43 along with C19 and R36 adjust the free-running frequency of the vertical oscillator to the point that it can lock to the **VS**SYNC signal. C28 is connected to the oscillator circuit by jumper W2-B for 50Hz screen refresh operation. The refresh rate is controlled by the **VS**SYNC from the logic board. Normally this jumper will be in the A position and C28 is not in the circuit.

R43 is adjusted to stop vertical roll by synchronizing the oscillator frequency with the vertical sync pulse (VSYNC).

The oscillator provides a vertical drive sawtooth signal, from U3, pin 5 for the vertical amplifier section.

DC feedback from the Vertical Amplifier section is input to U3, pin 3 for vertical position stability. AC feedback from the Vertical Amplifier section is input to U3, pin 4 for vertical size control.

The vertical amplifier section circuitry provides amplification of the vertical drive sawtooth signal for linear control of the current through the vertical deflection yoke. The amplifier section is similar to circuitry used in audio amplifiers. Circuitry consists of transistors Q20, Q21, Q6, Q7, Q3, and Q4, and potentiometers R143, and R134 with associated components.

With no current flowing through the vertical deflection coils, the beams from the CRT cathodes would strike the CRT at the center of the screen. The deflection coils, when current flows through them, function like an electromagnet, deflecting the beams to the top or bottom of the screen. The direction of current flow determines to which end of the screen the beams are deflected, while the amount of current determines how far the beams are deflected. The rate of change of the current flow controls the velocity of the movement. Current flow of a constant value would deflect the beams to the top or bottom of the screen and hold them there until the current flow changes direction or value.

With this information in mind, it can be determined that an alternating current (that which changes direction and value) would drive the beams from the center to the top or bottom of the screen, back to center and then to the other end of the screen.

Vertical drive sawtooth from the Vertical Oscillator U3, pin 5 is rising from a negative to a positive direction. Transistor Q20 inverts the vertical ramp.

When the beams from the CRT cathodes are at the top of the screen, the ramp is just beginning. Transistor Q7 is full on and biases transistor Q6 on. Transistors Q21, Q3, and Q4 are biased for minimum conduction. Capacitors C81 and C80 charge toward the +28VDC sourced through Q6. Current flow is from ground through R140, C80 and C81, the vertical yoke, diode CR3 to the +28VDC through Q6. Current flow through the yoke is maximum.

As the ramp progresses, Q6 begins to conduct less and Q4 begins to conduct. Q4 provides another path for current to flow from ground. At the same time the effects of the +28 VDC are diminishing because Q6 is conducting less. The amount of current flowing through the yoke decreases at a constant rate and the raster scans toward the center of the screen.

When the raster is at the center of the screen, Q4 and Q6 are conducting equally and current flow through the yoke is minimum.

As Q4 begins to conduct more heavily, current (from ground) through Q4 begins flowing through the yoke in the opposite direction, discharging C80 and C81. Current flowing through the yoke in the opposite direction increases at a constant rate and the raster scans toward the bottom of the screen.

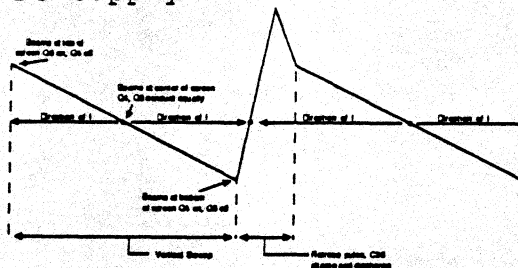
When the raster reaches the bottom of the screen, current flow through the yoke is maximum. Q6 is off and Q4 is on.

The vertical oscillator ramp signal at U3, pin 5, ends and quickly goes negative (retrace). Q4 turns off and Q6 turns on.

The energy stored in the deflection yoke attempts to sustain the direction of current flow. Capacitor C35 quickly charges to a positive potential (beginning of retrace pulse).

Once the energy from the deflection coil is spent on charging C35, current through the deflection coil very quickly stops and the raster is driven to the center of the screen. The positive charge on C35 discharges and draws maximum current from ground through C81 and C80, reversing current flow through the yoke and the raster is driven up and off the screen. When C35 discharges to equal the source voltage of Q6, the current through the yoke is reduced and the raster is brought back to the top of the screen.

Once again current flow charges C80 and C81 through the yoke to Q6 and the +28 VDC supply.



Representative current waveform signal through coil.
(Not drawn to scale)

Capacitor C33 charges while Q6 is off and provides a "bootstrap" voltage during retrace to ensure that Q6 turns on quickly and Q4 turns off quickly.

DC feedback for the vertical oscillator is from the positive side of C81, C80. The DC level of the vertical output at U3, pin 5, decreases if the DC charge on the capacitors increases. AC feedback for the vertical oscillator is from the vertical size control, potentiometer R134. The amplitude of the vertical ramp from the oscillator U3, pin 5, increases if the AC feedback decreases.

Vertical centering circuit acts as a current source or current drain for the vertical deflection yoke. Transistors Q19, Q18, and their associated components do this job.

+28 VDC is applied to transistor Q19. Potentiometer R138 is adjusted to effectively raise the DC voltage at the yoke and at the top of C80 and C81. When Q19 conducts (source), the screen center moves down.

Q18 is connected to ground. Potentiometer R139 is adjusted to effectively lower the DC voltage at the yoke and top of C80, C81. When Q18 conducts (drain), the screen center moves up. Because Q18 and Q19 signals cancel each other, only one transistor circuit should be adjusted for screen centering. The other should be adjusted for minimum conduction.

Vertical retrace blanking circuitry provides the video board with a positive TTL pulse during vertical retrace. Also generated by this circuit is a pincushion blanking pulse used in the **Parabola Generation** circuit. Integrated circuit U1 and associated circuits provide this function.

A positive pulse is output from U3, pin 7 and input at U1, pin 10 during vertical retrace. U1 is a dual monostable multivibrator, 1/2 of which is used by the blanking circuitry.

Capacitor C3 and resistor R8 determine the pulse width of the outputs on pin 5 (positive pulse to the video board via J4, pin 2) and pin 12 (negative pulse to the parabola generation circuit).

Horizontal centering circuitry receives the low true horizontal sync pulse (input at J2, pin 2) and provides an adjustable delay of the pulse for the **Automatic Frequency Control (AFC)** circuitry. This pulse is also used as a power supply sync (output at J2, pin 3). Circuitry consists of 1/2 of U1, U2 and associated circuitry.

Diodes CR1 and CR2 clamp noise spikes to keep the HSYNC signal at TTL levels. U1 and U2 are dual monostable multivibrators.

1/2 of U1, resistor R2 and capacitor C4 provide 2/3 cycle delay of the HSYNC pulse (input at pin 1, output at pin 13).

The first half of U2, potentiometer R10 and capacitor C7 provide an additional 0-2/3 cycle (adjustable) delay of HSYNC pulse (input at pin 1, output at pin 13).

The second half of U2, resistor R12 and capacitor C6 determine the pulse width (4us) of the delayed HSYNC pulse, now called PSSYNC (input at pin 9, output at pin 5).

Horizontal oscillator and AFC circuitry generates the horizontal drive signal synchronized with the HSYNC. An Automatic Frequency Control circuit (AFC, incorporated into U3) compares the Vertical Retrace pulse with the PSSYNC pulse and provides phase locked loop (PLL) control for horizontal stability. "Circuits" include U3, transistor Q5, potentiometer R25 and associated circuits.

Timing circuitry, capacitor C15, resistor R26 and potentiometer R25, allow adjustment of the horizontal oscillator output frequency. A saw-tooth waveform is developed across C15.

The horizontal oscillator output (U3, pin 9) is inverted by Q5 and passed on to the Driver circuits (on sheet two of schematic).

Resistor R60 (on sheet two of schematic) and capacitor C12 integrate the horizontal retrace pulse (derived from the horizontal drive signal) into a saw-tooth waveform. The retrace saw-tooth is input to U3, pin 13.

The PSSYNC pulse (derived from the HSYNC) is input to U3, pin 12.

The horizontal oscillator is adjusted so the center of the rising edge of the retrace saw-tooth meets the leading edge of the PSSYNC pulse.

AFC PLL operation:

The DC output (U3, pin 14) of the AFC circuit increases if the leading edge of the PSSYNC pulse is ahead of the center of the rising edge of the retrace saw-tooth. The DC output decreases if the PSSYNC trails the retrace saw-tooth.

U3, pin 14 output is used as feedback to the horizontal oscillator (U3, pin 10).

A rise in DC voltage at U3, pin 10 increases the oscillator frequency, effectively moving the retrace saw-tooth (U3, pin 13) to the desired position. The oscillator frequency decreases if the DC voltage at pin 10 decreases.

A positive voltage from the X-Ray protect circuits, (sheet two of schematic) input to U3, pin 8, shuts down the horizontal oscillator when the high voltage at the CRT anode exceeds a preset limit. Capacitor C17 filters noise that may accidentally trigger the horizontal oscillator to stop.

High Voltage saw-tooth circuitry provides a saw-tooth signal for the high voltage regulator. Integrated circuit U4 and associated components amplify the Horizontal Oscillator timing signal.

The input (U4, pin 5) for the HV saw-tooth circuitry is the horizontal saw-tooth timing signal. U4, a dual stage operational amplifier, amplifies the timing saw-tooth signal.

Capacitor C31 and resistor R41 form a band pass filter between the amplifier stages of U4. The HV saw-tooth is output (U4, pin 1) to the High Voltage Regulator (U7, pin 8) circuitry (sheet two of schematic).

Refer to SHEET TWO of schematic:

Driver circuits amplify the Horizontal Oscillator output and drive the primary of transformer T1. Circuitry consists of transistor Q9, and transformer T1, with associated circuitry.

Transistor Q9 amplifies the output of the horizontal oscillator, inverts the signal and drives the primary of transformer T1.

Secondary windings of T1 provide signals to three places.

1. Horizontal output section
2. High voltage regulator
3. CRT heater circuits.

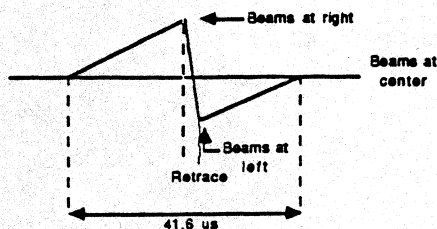
Horizontal output circuitry provides an alternating current ramp with slow linear rise time and fast fall time to drive the horizontal deflection yoke. The horizontal deflection circuitry also provides the **Horizontal Protection** circuits with some AC voltage and a retrace pulse for the **AFC** circuits. Transistor Q8, diode CR4, inductors L1 and L2, and resistor R69 and other components form this circuit.

With no current flowing through the horizontal deflection coils, the beams from the CRT cathodes would strike the CRT at the center of the screen. The deflection coils, when current flows through them, function like an electromagnet, deflecting the beams to either side of the screen. The direction of current flow determines to which side of the screen the beams are deflected, while the amount of current determines how far the beams are deflected. The rate of change of the current flow controls the velocity of the movement. Current flow of a constant value would deflect the beams to either side of the screen and hold them there until the current flow changes direction or value.

With this information in mind, it can be determined that an alternating current (that which changes direction and value) would drive the beams from the center to either side of the screen, back to center and then to the other side of the screen.

The alternating current, in an AR-2 deflection assembly, has a cycle time of about 41.6 microseconds, corresponding to a sweep rate of 24 kHz. At the beginning of a cycle, the current starts increasing linearly from zero to its peak value. As it does so, the beams are deflected from the center of the screen to the right side at a constant velocity. The current then changes direction very quickly, going from its peak positive value to its peak negative value in about 4.5 microseconds. The beams are deflected to the left side of the screen very quickly. This is called the "retrace" scan. At this point, the current through the yoke begins decreasing linearly from its peak negative value back to zero, and the beams are deflected to the center of the screen again. The process continues, with current changing directions and linearly increasing to its peak positive value.

It can be seen that the deflection coil current has a relatively slow linear sawtooth or ramp waveform with a very quick transition from peak positive value to peak negative value.



AR-2 DEFLECTION

Transistor Q8 is switched on by the Driver circuits for a period slightly less than one half cycle of the horizontal frequency. Just before Q8 is turned on, current flow through the horizontal yoke is minimum and the beams are at the center of the screen. When Q8 is turned on, current begins to flow from Q8 through the yoke, discharging capacitor C47 (C47 was charged by a previous cycle). The resonant characteristics of the horizontal yoke circuit, (C47 and parallel components, inductor L2 and resistor R69) causes the charge and discharge of C47 to occur in a linear fashion. Current builds to its peak positive value while Q8 is turned on and the beams sweep at a linear rate to the right side of the screen.

When Q8 turns off, the energy stored in the horizontal yoke quickly charges capacitor C44. When C44 charges completely, current flow through the yoke stops. C44 quickly discharges and current through the yoke reverses and quickly climbs to its peak negative value. The resonant characteristics of the horizontal yoke circuit causes the charge and discharge of C44 to be very quick and the beams are swept from the right to the left side of the screen very quickly (retrace). As the CRT beams are returned during horizontal retrace, the sudden reversal of current flow in the deflection coil results in a large "flyback" pulse at the collector of Q8. This pulse is dampened by diode CR4. WERE CR4 NOT IN THE CIRCUIT THE PULSE WOULD DESTROY Q8.

After the retrace, C47 begins charging toward the supply voltage of the Horizontal Output Voltage Regulator and current through the yoke begins to decrease at a linear rate. The beams move at a constant rate back to the center of the screen.

The width of the scan is determined by the value of the supply voltage output from the Horizontal Output Voltage Regulator.

The retrace pulse is integrated into a sawtooth signal by resistor R60 and capacitor C12 (on sheet one of schematic), and input to the AFC PLL circuit of the Horizontal Oscillator, U3, pin 13.

The AC voltage of the Horizontal Deflection circuits is rectified by diode CR6 and filtered by capacitor C50 for detection of horizontal drive by the Horizontal Protection circuits.

Parabola and top corner correction circuits generate a vertical pincushion corrective signal for the Horizontal Voltage Regulator. Circuitry consists of U6, U5, and associated circuitry.

The output of the **Horizontal Deflection Regulator** determines the width of each horizontal sweep. Differences in the radius of the curvature of the screen and the radius of the curvature of the horizontal sweep would cause the sides of a display to curve inward at the center if the voltage supplied to the horizontal yoke is constant throughout a vertical sweep. By modulating the **Horizontal Deflection Regulator** so that the horizontal output is less at the beginning (top) and end (bottom) of the vertical sweep the sides of the display can be made straight.

U6 is configured as a multiplier circuit. The vertical ramp is input and multiplied by itself. The resultant signal is a parabola shaped voltage output.



A vertical ramp signal from the vertical deflection amplifier is input to U6, pins 4 and 9.

The input on U6, pin 12 is adjusted by potentiometer R114 to some voltage between +12 VDC and -12 VDC. R114 is adjusted for a symmetrical parabola output at U5, pin 7. U6 pin 8 is grounded.

The resultant signal of the multiplier circuit is output at U6 pins 14 and 2. The output of U6 is amplified by 1/4 of U5, a four stage differential amplifier. Input is on U5, pins 5 and 6.

Potentiometer R102 adjusts the feedback on U5, pin 6 to set the gain of the amplifier. The output (U5, pin 7) is a parabola shaped wave form.

The retrace pulse in the parabola must be cancelled out to prevent the horizontal deflection circuit from ringing and distorting the top corners of the display. Top corner correction is affected by 1/4 of U5 (input pins, 10 and 9) and potentiometer R120. Potentiometer R120 is adjusted for an output (U5, pin8) equal in amplitude but opposite in polarity to the retrace pulse in the parabola.

Diodes CR14 and CR15 act as an OR gate to pass both signals to the horizontal drive voltage regulator. The vertical retrace pulse occurs at the same time as the pulse from the top corner correction circuit and the two signals cancel each other out.

The parabola signal is used to modulate the Horizontal Output Voltage Regulator circuit so that the sides of the display are straight.

Horizontal output voltage regulator circuits provide the horizontal drive circuits with a regulated, pincushion corrected, voltage source. Horizontal screen size is set by adjustment of the regulator voltage. Circuitry consists of U5, transistors Q1, Q2, and Q17, potentiometer R24 and associated circuitry.

When transistor Q1 conducts, transistor Q2 conducts and provides the horizontal deflection circuits with a portion of B+ voltage from the power supply.

Feedback from emitter of Q2 is adjusted by potentiometer R124 to set the regulator voltage which controls the width of the display.

The pincushion parabola and feedback from Q2 are both input to 1/4 of differential amplifier U5, pin 13. The output of U5, pin 14 controls transistor Q17. The current path for Q17 is through horizontal protection circuitry (transistor Q10 and associated circuitry) to ground.

When Q17 conducts, voltage on the base of Q1 is less.

The feedback from Q2 and the parabola now control the **Horizontal Drive Voltage Regulator**. The B+ voltage is modulated by the pincushion parabola to increase the regulator voltage as the sweep approaches the middle of the screen.

High voltage regulator circuitry and the flyback transformer generate the 25 Kilo-volts for the anode of the CRT. High voltage soft start is also provided by this circuit. Circuitry consists of U7, transistors Q16, Q15, Q14, and Q11, potentiometer R89 and associated circuitry.

The HV circuitry is a switching type power supply, switched by a secondary of T1 (Driver signal). The HV saw-tooth signal and feedback from the flyback transformer provide pulse width voltage regulation.

U7 is a dual stage differential amplifier used for HV soft start and control of the HV regulator. High voltage soft start is initiated when power is first applied to the deflection board, U7, pin 3 is at -12 VDC potential. As capacitor C59 charges, pin 3 (non-inverting pin) rises toward ground potential, U7, pin 1 voltage also rises.

The output of U7, pin 1 is input to U7, pin 5. The HV saw-tooth is input to U7, pin 8. As the voltage on U7, pin 5 rises, more of the HV saw-tooth (U7, pin 8) pulse-width is output at U7, pin 7.

The output of U7, pin 7 controls inverting transistor Q16. Conduction path for Q16 is through the **Horizontal Drive Protection** circuits (Q10 and associated circuitry) to ground. The **Horizontal Drive Protection** circuit removes the conduction path for Q16 when horizontal drive is lost.

The voltage on the base of transistor Q15 goes low when Q16 is on. The conduction of Q15 lowers the base voltage of transistor Q14. Transistor Q14 provides the switching circuitry (through the flyback) with a portion of the B+ voltage from the power supply.

Transistor Q11 is switched on and off at the horizontal rate by the **Driver** signal from the secondary of T1. When Q11 is on, current flows through the flyback transformer and Q11 to ground.

When Q11 is turned off, capacitor C54 charges and discharges quickly through the flyback transformer creating a high voltage spike. Diode CR8, across C54, prevents oscillations in the flyback circuitry.

Internal diodes of the flyback transformer rectify the high voltage spikes into the DC voltage.

Positive DC feedback from the flyback transformer is an input at U7, pin 2. The DC feedback is inverted (U7, pin 1) and input to U7, pin 5.

An increase in the feedback voltage causes a lower voltage at U7, pin 5. A lower voltage at U7, pin 5 results in narrower pulses to Q16. Q16 allows less current to flow through the flyback transformer. Capacitor C54 charges to a smaller value.

Potentiometer R89 cancels some of the feedback signal to set the **High Voltage Regulator** at the desired voltage output. Usually 25 KV at the anode cap.

Automatic control of the pulse-width modulation (via feedback) regulates the output high voltage.

Horizontal protection circuitry shuts down the **High Voltage Regulator** and the **Horizontal Drive Voltage Regulator** when horizontal deflection drive is lost. Circuitry consists of diode CR6, capacitor C50, transistor Q10 and associated circuits.

Transistor Q10, when biased on, provides a path for current flow for **Horizontal Drive Voltage Regulator** transistor Q17 and **HV Regulator** transistor Q16.

When power is first applied to the deflection board, capacitor C53 conducts current from B+ to the base of Q10 and begins to charge. The charge time is set by the value of C53 and resistors R63, R61, and R62.

C53 conducts long enough for a portion of the horizontal deflection AC signal to charge capacitor C50 with a positive voltage. Diode CR6 provides positive pulses for C50.

C50 discharges and Q10 turns off when the horizontal deflection signal is lost. The **High Voltage Regulator** and the **Horizontal Output** circuitry is shut down when Q10 turns off.

X-Ray protection circuit shuts down the **Horizontal Oscillator** if the high voltage exceeds 29 KVDC. Circuitry consists of U5, diode CR20, potentiometer R103 and associated circuits.

A sample of the flyback signal is output at pin 5 of the flyback transformer and rectified by diode CR13 charging capacitor C58 to a negative voltage. This voltage passes through a voltage divider, consisting of resistors R86, and R105 and potentiometer R103.

Potentiometer R103 provides an adjustable positive off-set voltage tied to U5, pin 2 to adjust the **X-Ray protect** circuitry.

The output of U5, pin 1 is low in normal operation. When the HV exceeds the desired level, the voltage on U5, pin 2 is inverted and shuts down the horizontal oscillator.

Flyback transformer provides the CRT anode with the 25KV high voltage, the G1 (control grid) **Voltage Regulator** with negative supply voltage, and feedback for the **High Voltage Regulation** circuits. The flyback also allows G2 (screen grid) and **focus** control.

Grid 1 voltage regulator circuits provide a regulated negative bias voltage for the control grid (G1) of the CRT. Circuitry consists of diode CR13, capacitor C58, transistors Q13 and Q12 and associated circuits.

Diode CR13 provides negative pulses for capacitor C58 to develop a negative DC charge.

When transistor Q12 conducts, transistor Q13 conducts and provides a portion of the negative charge on C58 to G1, output at J4, pin 3. Zener diode CR10 provides regulation of Q12 emitter voltage to 6.3 VDC. An external brightness potentiometer (connected to the circuit by J6) controls the base bias of Q12 and the output of Q13.

Automatic Beam Current Limiting (ABL) circuits provide the video board with a negative voltage which represents the amount of current through the flyback. Circuitry consists of potentiometer R78, capacitor C56 and associated circuits. The ABL is sometimes called Extended High Voltage Regulation (EHVR).

Negative pulses from the flyback transformer develop a negative DC voltage on capacitor C56. Resistor R77 and potentiometer R78 set the voltage on C56 by shunting a selected portion of the signal to ground.

A maximum current of 400 micro-amps is desired to protect the CRT.

The negative voltage to the video board decreases the output of the video drivers when the maximum current is reached. When video driver output is reduced, flyback current is also reduced.

CRT heater and Status Indicator circuitry develops an ac voltage for the CRT heater and status lamp. The status indicator lamp will light when the HV circuitry is operating correctly. Circuitry consists of part of T1, diode CR9, and associated circuitry.

A secondary of T1 provides part of the base driver AC signal to power the CRT heater filament. Output at J4, pins 4 and 5.

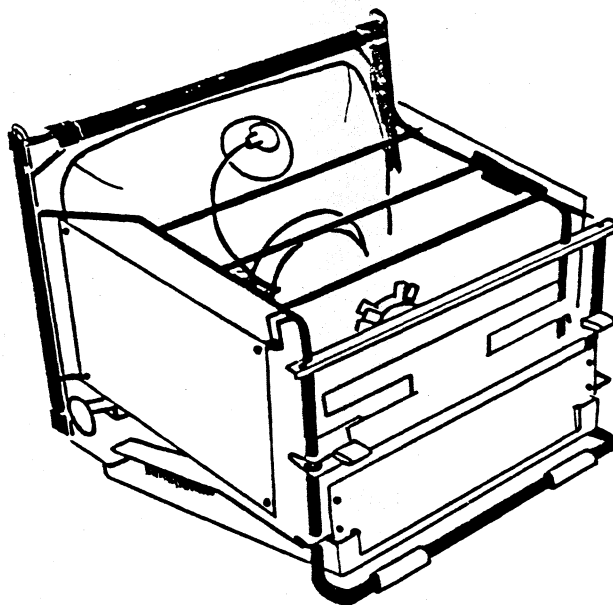
Diode CR9 provides some DC voltage to the status indicator lamp. Output J6, pins 1 and 2.

THE STATUS INDICATOR LAMP IS NOT A POWER ON INDICATOR!! It IS an indication of a failure in the Horizontal Oscillator or Horizontal Output circuits.

THE VIDEO BOARD

The Video Amplifier converts the Red, Green, and Blue (TTL level) video signals from the logic board into cathode drive signals for the CRT. The Video assembly contains three separate amplifiers, each with a digital to analog converter and a two stage amplifier. Other circuitry on the board provides Automatic Beam Current Limiting (ABL), and Vertical Retrace Blanking.

The video board is located at the rear of the unit, mounted to the frame with four machine screws.



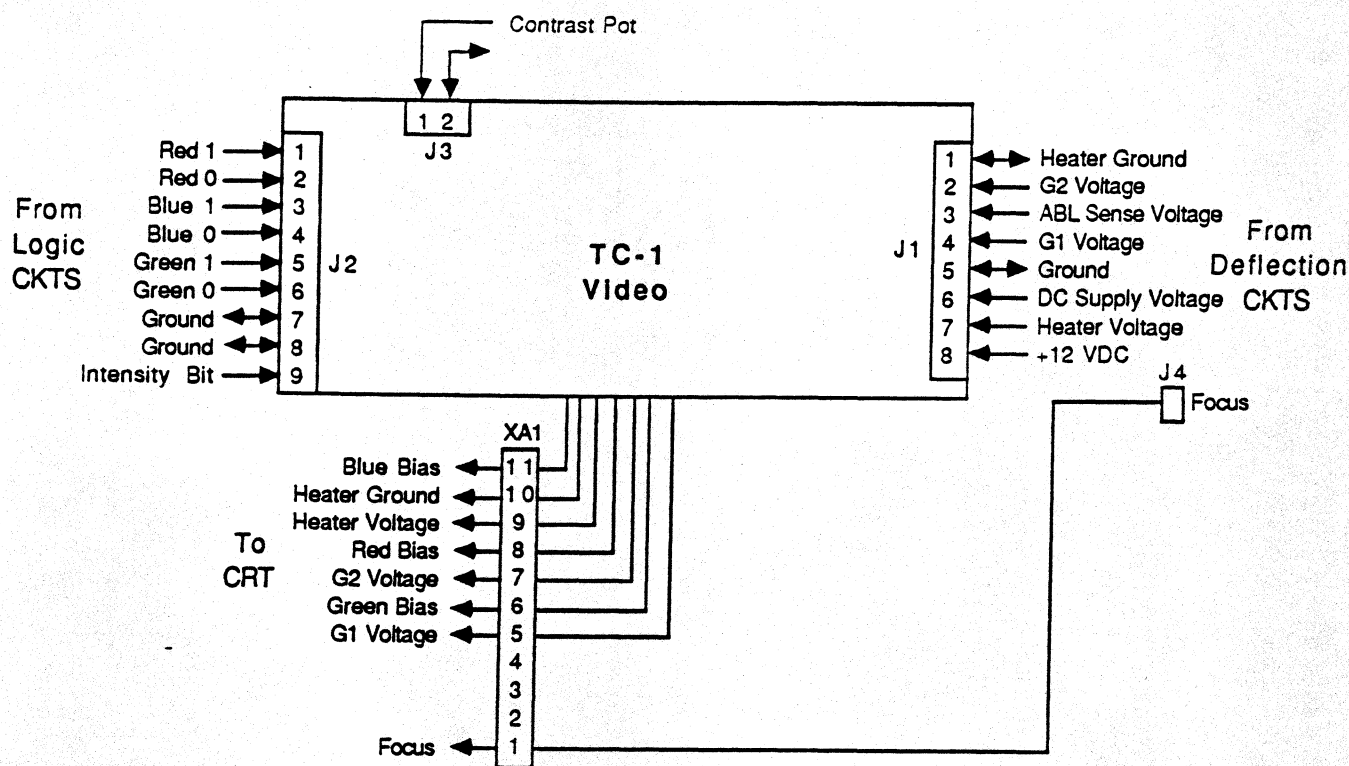
Identification of the Video boards and relative schematics are shown below.

		Schematic	Board
3800	TC-1 Video	# 105110	# 105112
8800	TC-3 Video	# 105200	# 105202
8800	AR-2 Video	# 105197	# 105199

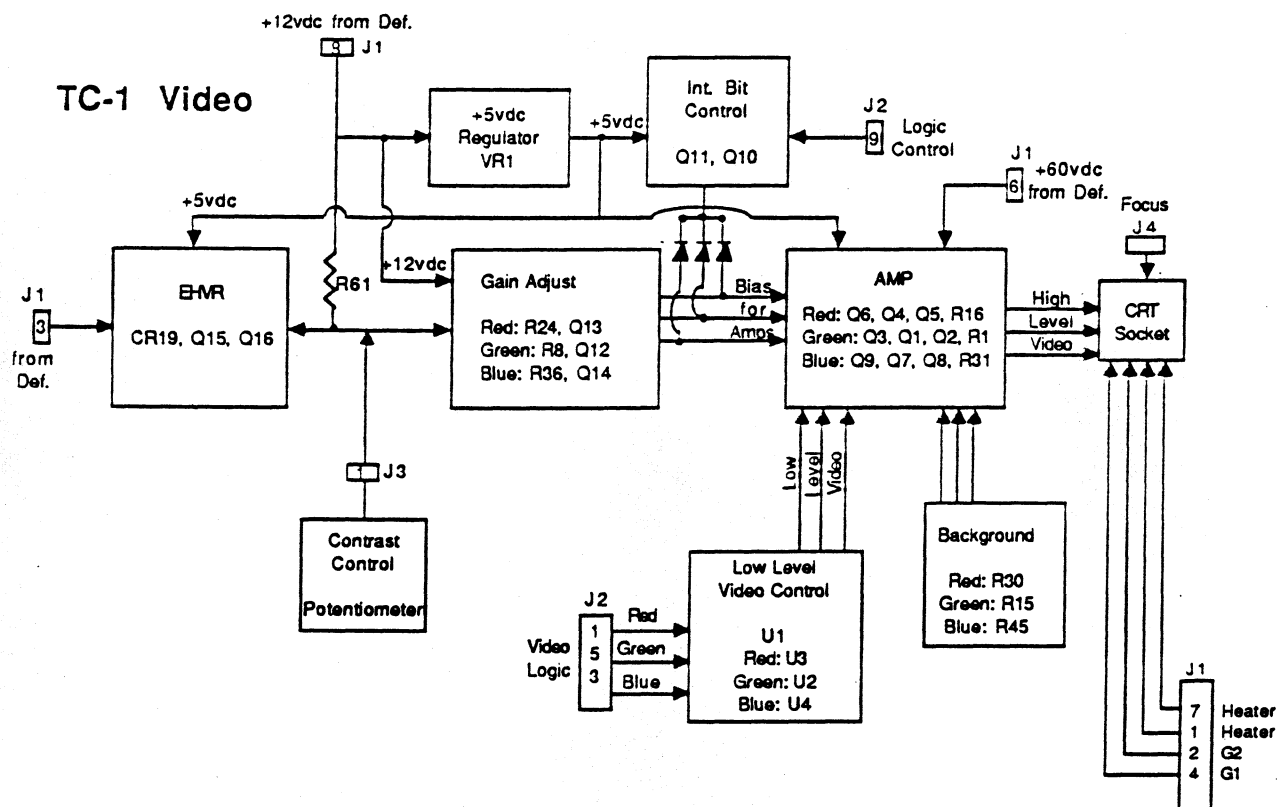
TC-1 VIDEO AMPLIFIER

Refer to schematic drawing #105110 rev 3 or later and the block diagram for the TC-1 video.

The TC-1 video amplifier board consists of three digital video driver channels. The amplifier channels are designed to accept one or two bit TTL digital input and provide drive to the CRT cathodes. Each amplifier has gain and bias adjustments to allow balancing of background and drive levels to the individual guns of the CRT.

Input and Output Wiring

BLOCK DIAGRAM

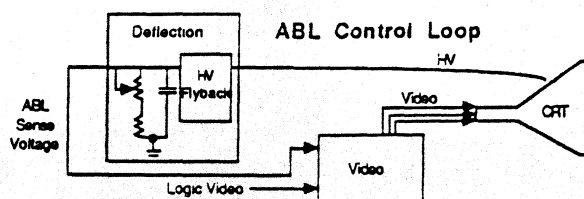


Board #105112
Schematic #105110

Circuit Description:

Video Gain Bus voltage through resistor R61 is used by the three **Gain Adjust** sections to set the gain of each amplifier. Any change in this voltage will affect all three amplifiers simultaneously.

Automatic Beam Current Limiting (ABL), also called Extended High Voltage Regulation (EHVR), circuitry automatically controls the gain of each amplifier section to limit the amount of current drawn by the cathodes of the CRT to some pre-set value. Transistors, Q16 and Q15, and diode CR19 with associated circuitry perform this function.



A current control loop is established by the ABL circuitry on the deflection board and the video board. The negative ABL sense voltage, input at J1, pin 3, represents the amount of current flowing through the high voltage flyback transformer. When this voltage exceeds about -7.5 VDC, zener diode CR19 starts to conduct and biases transistor Q15 on.

Q15 conducts and biases transistor Q16 on. The Video Gain Bus voltage is reduced when Q16 conducts. When the gain of the video amplifier is reduced, the CRT cathode voltage is increased (screen intensity decreases) and current through the HV flyback transformer is reduced.

A voltage through resistor R54 charges capacitor C16 and biases Q15 off when the current through the flyback transformer does not exceed the set limit.

C16 slows the response of the ABL circuitry to allow short duration, high peak, beam currents to occur. C16 also eliminates oscillation of the ABL system.

Contrast Control circuitry provides an external control of the Video Gain Bus voltage. An external 1K potentiometer is connected at J3, pins 1 and 2 in parallel with the output of the ABL circuitry.

Resistors R61, and R60, and the external contrast potentiometer form a voltage divider which controls the Video Gain Bus voltage.

Intensity Bit circuitry provides a way to modulate the output of all three video amplifiers simultaneously. The logic board in 3800 and 8800 terminals does not generate an intensity bit. However, if this circuitry fails, problems may develop in the amplifier and the circuit description will be discussed. Transistors Q11 and Q10, diodes CR5, CR9, CR13, CR17, and other associated circuitry form this circuit.

A "low" input to J2, pin 9 biases Q11 on, which biases transistor Q10 on. When Q10 conducts, CR5, CR9, and CR13 are forward biased and the base bias voltage to the first stage amplifier of each Amplifier Control section is reduced at the same time.

Since the three video amplifier circuits are identical, only the Red channel is described below. Corresponding components, in the Green and Blue circuitry, perform identical functions.

Low Level Video Drive circuits (when processing one bit video) act as an "on/off" switch controlled by the Logic board, for the **Amplifier Control** section. Integrated circuits U1, and U3 with associated circuitry, provide this function.

Low true TTL video logic is input to J2, pin 1. Jumper W1 should be installed to process the one bit video information from Intecolor 3800 series logic. A 74S04 buffer IC, U1, inverts the input and protects the logic from damaging noise spikes that may be present in the video amplifier circuitry.

When ground, or a "low", is applied to the inputs of U1, its outputs go "high". NAND gate U3, a 74S38 IC, inverts the signal from U1 and provides a low impedance path for current to flow from ground to the first stage amplifier of the **Amplifier Control** section. If the input to U1 goes "high" or opens, its output pins go low and U3 removes the path for current flow.

Resistors R25, R27, and R28 provide "weighting" of the current path from ground when the board is used for "two bit" video processing. The value of these resistors was selected to make the video output colors match industry standards.

Schottky ICs are used to provide the fast turn-on and turn-off necessary to achieve the sharp rise and fall times at the output of the amplifier.

Gain Adjust circuitry sets the gain of the video amplifier.

Transistor Q13, potentiometer R24, and associated circuitry provide this function.

The **Video Gain Bus** voltage from R61 is adjusted, by potentiometer R24, to control the base bias of transistor Q13. Q13 buffers gain control, R24, to provide a low impedance voltage source for the common base, first stage amplifier Q6, of the **Amplifier Control** section.

Diode CR9 prevents the bias voltage of the red amplifier stage from affecting any other stage.

The output of the gain adjust is a positive voltage on the base of transistor Q6.

Background circuitry provides an adjustable resistance to ground for the first stage amplifier Q6, of the **Amplifier Control** section. Circuitry consists of resistor R29 and potentiometer R30.

Current flow through Q6 controls the output of the amplifier. Potentiometer R30 and resistor R29, allows adjustment of the current flow through Q6.

With no video enabled, the output of the amplifier is adjusted to bias the CRT cathode at just below conduction.

Amplifier Control circuitry provides amplification of the **Low Level Video Drive** signal, impedance matching to the CRT and buffers the low voltage circuitry from the CRT. Components in the Amplifier section are; transistors Q6, Q4, and Q5, inductors L5 and L2, diodes CR6, CR7, CR15, resistor R16 and associated components.

Video amplification is provided by a two stage amplifier. The first stage is common base amplifier, transistor Q6, and the second stage is a "push-pull" amplifier, complementary transistors Q4 and Q5.

The base of Q6 is biased to some positive DC voltage by the **Gain Adjust** circuits. Current flow for Q6 is from ground (controlled by the **Background** or **Low Level Video Drive** circuits) through Q6, diodes CR7, and CR6, inductor L5 and resistor R16 to the +60 VDC provided by the deflection board.

Q4 and Q5 form a push-pull amplifier to drive the cathodes of the CRT. Current flow through the push-pull amplifier is from ground through resistor R21, Q5, resistors R20 and R18, Q4, and resistor R17 to the +60 VDC supply. The output voltage to the cathode of the CRT is from common point of R18 and R20 through inductor L2.

Base bias voltage of Q4 and Q5 is controlled by the current flow through Q6. Diodes CR6 and CR7 each provide one diode voltage drop to compensate for voltage drops of Q4 and Q5 and insures that the "push-pull" transition of the amplifier is linear.

With no "Red" video enable, the **Background** circuits (R30) allow some current to flow from ground, through Q6, to the positive collector supply voltage.

When R30 is adjusted for minimum current flow, the collector voltage of Q6 is high. Base bias on Q4 and Q5 is high positive voltage. Transistor Q4 is biased on and Q5 is biased off. The output voltage of the amplifier is near the +60 VDC supply voltage and the cathode of the CRT is biased off.

When R30 is adjusted for maximum current flow, the collector of Q6 drops. Base bias of Q4 is about 1.2 VDC higher than Q5. Transistor Q4 is biased less and Q5 is biased on. The output voltage of the amplifier is less than the +60 VDC supply voltage and the cathode of the CRT is biased on.

R30 is adjusted so the output voltage is low enough to bias the CRT cathode just below conduction.

When the "Red" video is enabled, the low impedance path to ground (provided by U3) causes Q6 to increase conduction and its collector voltage drops. The base bias of Q4 is reduced and the base bias of Q5 is increased. The output voltage of the amplifier decreases by about 30 volts and the CRT cathode is biased on.

Diode CR15 shunts high positive pulses that may be generated by CRT arcs to the +60 VDC supply.

Inductor L5 peaks the collector circuit of Q6 for enhanced rise and fall time.

Inductor L2 resonates with the CRT capacitive load to provide improved rise and fall time at the CRT.

Resistor R16 must be an Allen Bradley type to assure proper tube arc protection characteristics.

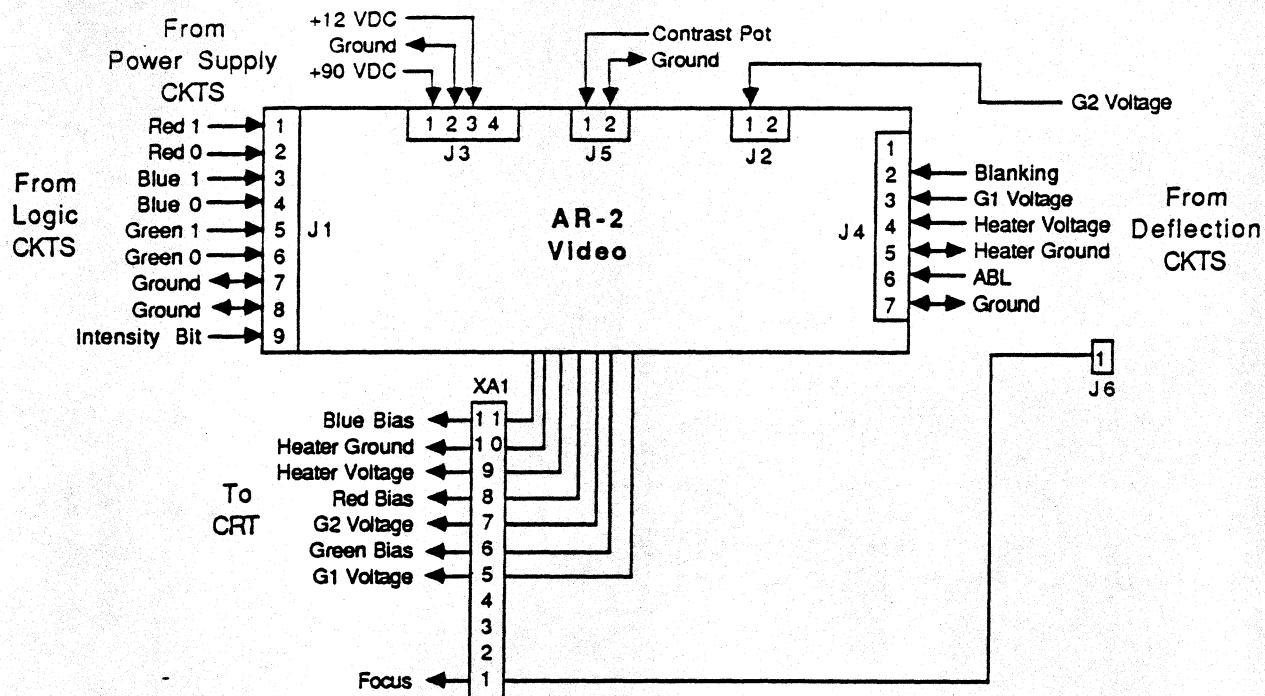
Diode CR8 shunts pulses more positive than +5 VDC to the +5 volt regulator to protect U3.

AR-2 VIDEO AMPLIFIER

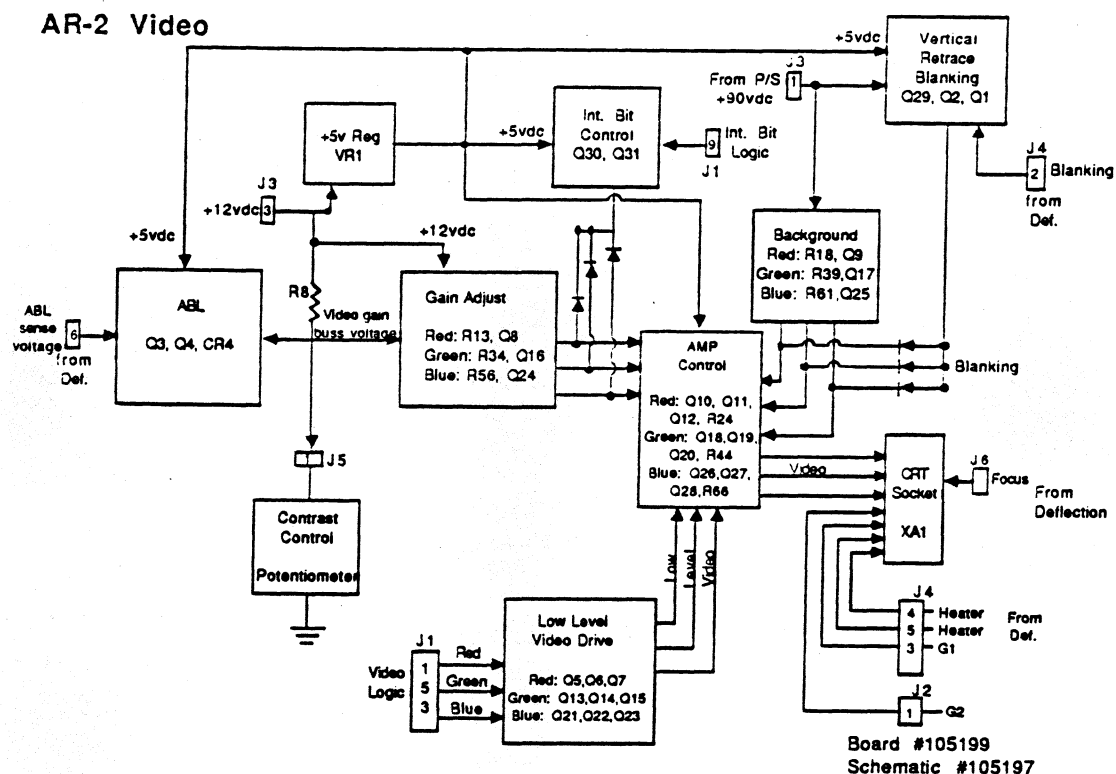
Refer to schematic drawing #105197 rev 1 or later and the block diagram for the AR-2 video.

The AR-2 video amplifier board consists of three digital video driver channels. The amplifier channels are designed to accept one bit TTL digital input and provide drive to the CRT cathodes. Each amplifier has gain and bias adjustments to allow balancing of background and drive levels to the individual guns of the CRT.

Input and Output Wiring

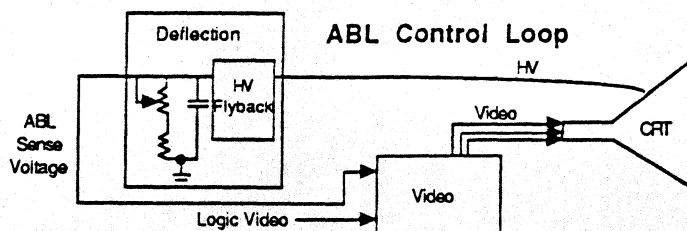


BLOCK DIAGRAM

**Circuit Description:**

Video Gain Bus voltage through resistor R58 is used by the three **Gain Adjust** sections to set the gain of each amplifier. Any change in this voltage will affect all three amplifiers simultaneously.

Automatic Beam Current Limiting (ABL), circuitry automatically controls the gain of each amplifier section to limit the amount of current drawn by the cathodes of the CRT to some pre-set value. Some of the components in this circuitry are, transistors, Q3 and Q4, and diode CR4.



A current control loop is established by the ABL circuitry on the deflection and the video board. Circuitry on the deflection board develops a negative voltage, input at J4, pin 6, that represents the amount of current flowing through the high voltage flyback transformer. When the flyback current produces a voltage which exceeds about -7.5 VDC, zener diode CR4, starts to conduct and biases transistor Q3 on.

Q3 conducts and biases transistor Q4 on. The Video Gain Bus voltage is reduced when Q4 conducts. When the gain of the video amplifier is reduced, the cathode bias voltage is increased, display intensity is decreased and current through the HV flyback transformer is reduced.

A voltage through resistor R72 charges capacitor C8 which biases Q3 off when the current through the flyback transformer does not exceed the set limit.

Capacitor C8 slows the response of the ABL circuitry to allow short duration, high peak, beam currents to occur. C8 also eliminates oscillation in the ABL system.

Contrast Control circuitry provides an external control of the Video Gain Bus voltage. An external 1K potentiometer is connected at J5, pins 1 and 2 in parallel with the output of the ABL circuitry.

Resistors R58, and R59, and the external contrast potentiometer form a voltage divider which controls the Video Gain Bus voltage.

Intensity Bit circuitry provides a way to modulate the output of all three video amplifiers simultaneously. The Logic board of 3800 and 8800 Series terminals does not generate an intensity bit. Problems could develop in the amplifier if the Intensity Bit circuitry fails, therefore circuit description will be discussed. Transistors Q30 and Q31, diodes CR8, CR17, CR27, CR35, and other associated circuitry are parts of this circuitry.

A "low" input to J1, pin 9 biases Q30 on, which puts a positive voltage on the base of transistor Q31. When Q31 conducts, CR8, CR17, and CR27 are forward biased and the base bias voltage of the first stage amplifier in each Amplifier Control section is reduced at the same time.

Vertical Retrace Blanking circuitry simultaneously shuts off, or "Blanks", the output of all three video amplifiers during vertical retrace. Circuitry consists of transistors Q29, Q2, and Q1, diodes CR2, CR9, CR26, CR1, CR22, and CR34, and associated circuitry.

A positive TTL pulse is generated, in the AR-2 deflection circuitry, for every vertical retrace and input to the video board at J4, pin 2. Diode CR1 limits the input to +5 VDC.

Transistor Q29 is in parallel with each background circuit and is biased off by +90 VDC through resistor R36 when transistor Q2 is off.

The collector of transistor Q1 is tied to +5 VDC. During each vertical retrace pulse, Q1 conducts and biases Q2 on. When Q2 conducts the base of Q29 is pulled toward ground and Q29 is biased on. Q29 bypasses each background circuit through diodes CR2, CR9, and CR26 and increases the base bias voltage to the second stage of the Amplifier Control circuitry.

Raising the voltage at this point, effectively increases the bias voltage on each cathode of the CRT (CRT intensity is decreased). Refer to Amplifier Control section circuit description below to see how this is done.

Diode CR22 protects Q1 and the deflection circuitry should Q2 fail (short).

The three video amplifier circuits are identical. Only the Red channel is described below. Corresponding components, in the Green and Blue circuitry, perform identical functions.

Low Level Video Drive circuits, create a high speed "on/off" switch for the Amplifier Control section. Transistors Q5, Q6, and Q7, and associated components provide this function.

A low true TTL waveform with logic high greater than +2.4 volts and logic low of less than +.4 volts is input to J1, pin 1. Diodes CR5 and CR6 limit input to TTL voltage levels. Transistor Q5 is biased to operate as an inverting saturated amplifier. Q5 converts the somewhat ragged TTL waveform from the logic into a clean waveform with fast rise and fall times.

The emitter of Q5 is biased one diode drop (approximately .65 Volts) above ground by diode CR7. The voltage required to bias Q5 on must exceed two diode voltage drops (voltage drop of CR7 and Q5) or +1.3 VDC. This guarantees complete turn off of Q5 when the input drops to TTL low, preventing ringing noise from appearing in the output. The nominal +2.4 VDC TTL input biases Q5 near saturation.

Transistor Q6 provides current gain and level shifting to turn transistor Q7 on and off rapidly. Q6 is an emitter follower and is biased on when Q5 is biased off. The high current gain of Q6 sources to the base of Q7 adequate current to drive Q7 on quickly, while resistor R12 is low enough impedance to discharge base to emitter capacitance of Q7 quickly for fast turn off. Base to emitter drop of Q6 level shifts base voltage of Q7 to assure turn off of Q7 when Q5 is turned on.

Q7 is biased as a saturated common emitter amplifier. Note that the same diode, CR7, is used to bias the emitters of both Q5, and Q7 above ground. Q5 is an inverting transistor driving Q7 through an emitter follower, so only one transistor, Q5 or Q7, is drawing current through the diode at a time. The effective resistance of CR7 provides some positive feedback between the saturated stages which ensures fast turn on and turn off.

Gain Adjust circuitry sets the gain of the video amplifier. Transistor Q8, potentiometer R13, and associated circuitry provide this function.

The **Video Gain Bus** voltage from R58 is adjusted, by potentiometer R13, to control the base bias of transistor Q8. Q8 buffers gain control, R13, to provide a low impedance voltage source (base bias) for transistor Q10, the first stage amplifier of the **Amplifier Control** section.

Diode CR8 prevents the bias voltage of the red amplifier stage from affecting any other stage.

The output of the gain adjust is some positive voltage on the base of transistor Q10.

Background circuitry provides an adjustable base bias voltage for the second stage amplifier in the **Amplifier Control** section. This circuitry is used to bias the cathodes of the CRT at just below conduction. Circuitry consists of transistor Q9, diode CR3, potentiometer R18, and associated circuitry.

The collector of transistor Q9 is tied to +90 VDC and potentiometer R18 sets the bias on the base of Q9. Resistor R17 limits the bias of Q9 and insures that the output of the **Vertical Retrace Blanking** circuitry is a minimum of +10 VDC greater than the output of the **Background** circuitry.

Diodes CR3 and CR2 prevent the output of the red background circuitry from affecting the other two background circuits through the **Vertical Retrace** circuitry.

Amplifier Control circuitry provides amplification of the Low Level Video Drive signal, impedance matching to the CRT and buffers the low voltage circuitry from the CRT. Components in the Amplifier Control section are transistors Q10, Q11, and Q12, inductors L1 and L2, diodes CR10, CR11 and CR12, resistor R24 and associated components.

Video amplification is provided by a two stage amplifier. The first stage is common base amplifier, transistor Q10, and the second stage is a "push-pull" amplifier, complementary transistors Q11 and Q12.

The base of Q10 is biased to some positive DC voltage by the Gain Adjust circuits. Current flow for Q10 is from ground through the Low Level Video Drive circuits, Q10, diodes CR11, and CR10, inductor L1 and resistor R24 to the Background circuits.

Q11 and Q12 form a push-pull amplifier to drive the cathode of the CRT. Current flow through the push-pull amplifier is from ground through resistor R28, Q12, resistors R27 and R26, Q11, and resistor R25 to the +90 VDC provided by the power supply board. The output voltage to the cathode of the CRT is from common point of R26 and R27 through inductor L2.

Base bias voltage of Q11 and Q12 is controlled by the current flow through Q10. Diodes CR10 and CR11 each provide one diode voltage drop to compensate for the voltage drops of Q11 and Q12 and insures that the "push-pull" transition of the amplifier is linear.

With no "Red" video enable, resistor R21 allows some current to flow from ground, through Q10, to the positive collector supply voltage.

Increasing the supply voltage of Q10 increases the bias of Q11 and reduces the bias of Q12. The output voltage of the amplifier goes more positive and the CRT screen intensity is decreased.

When the "Red" video is enabled, the low impedance path to ground, provided by Q7, causes Q10 to increase conduction and its collector voltage drops. Base bias of Q11 is reduced and base bias of Q12 is increased. The output voltage of the amplifier decreases by about 60 volts and the CRT cathode is biased on.

Diode CR13 shunts high positive pulses that may be generated by CRT arcs to the +90 VDC supply.

Inductor L1 peaks the collector circuit of Q10 for enhanced rise and fall time.

Inductor L2 resonates with the CRT capacitive load to provide improved rise and fall time at the CRT.

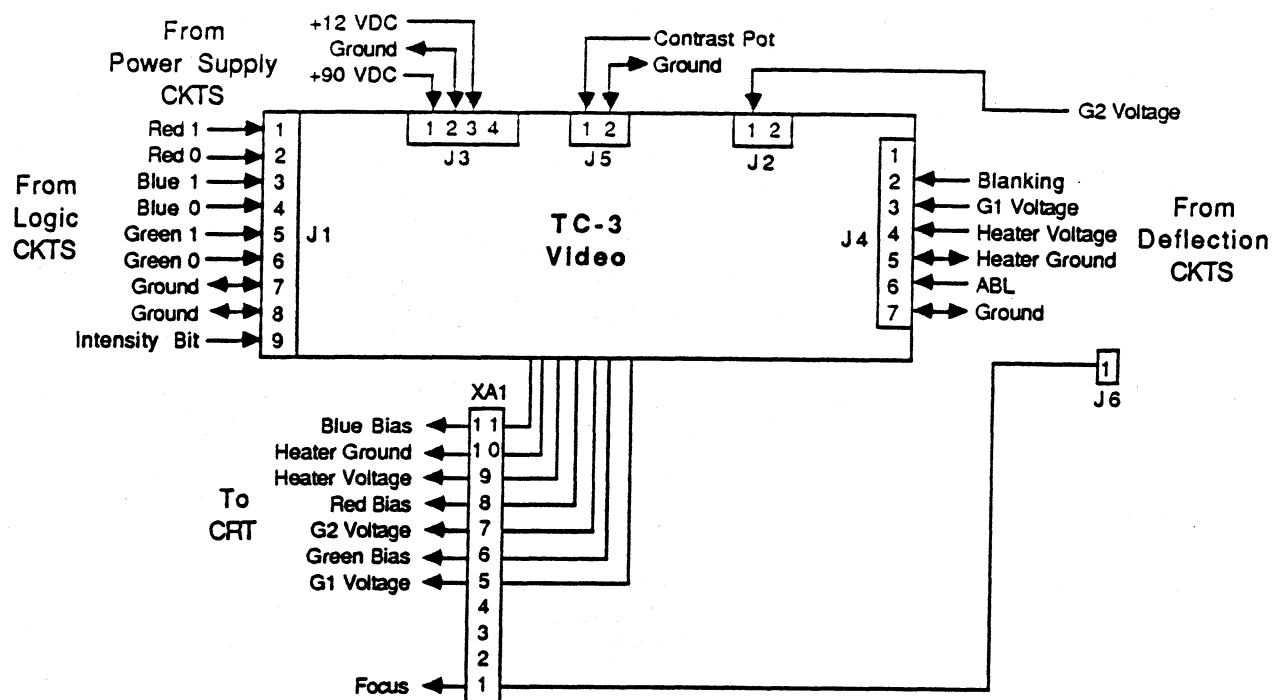
Resistor R24 must be an Allen Bradley type to assure proper tube arc protection characteristics.

TC-3 VIDEO AMPLIFIER

Refer to schematic drawing #105200 rev 1 or later and the block diagram for the TC-3 video.

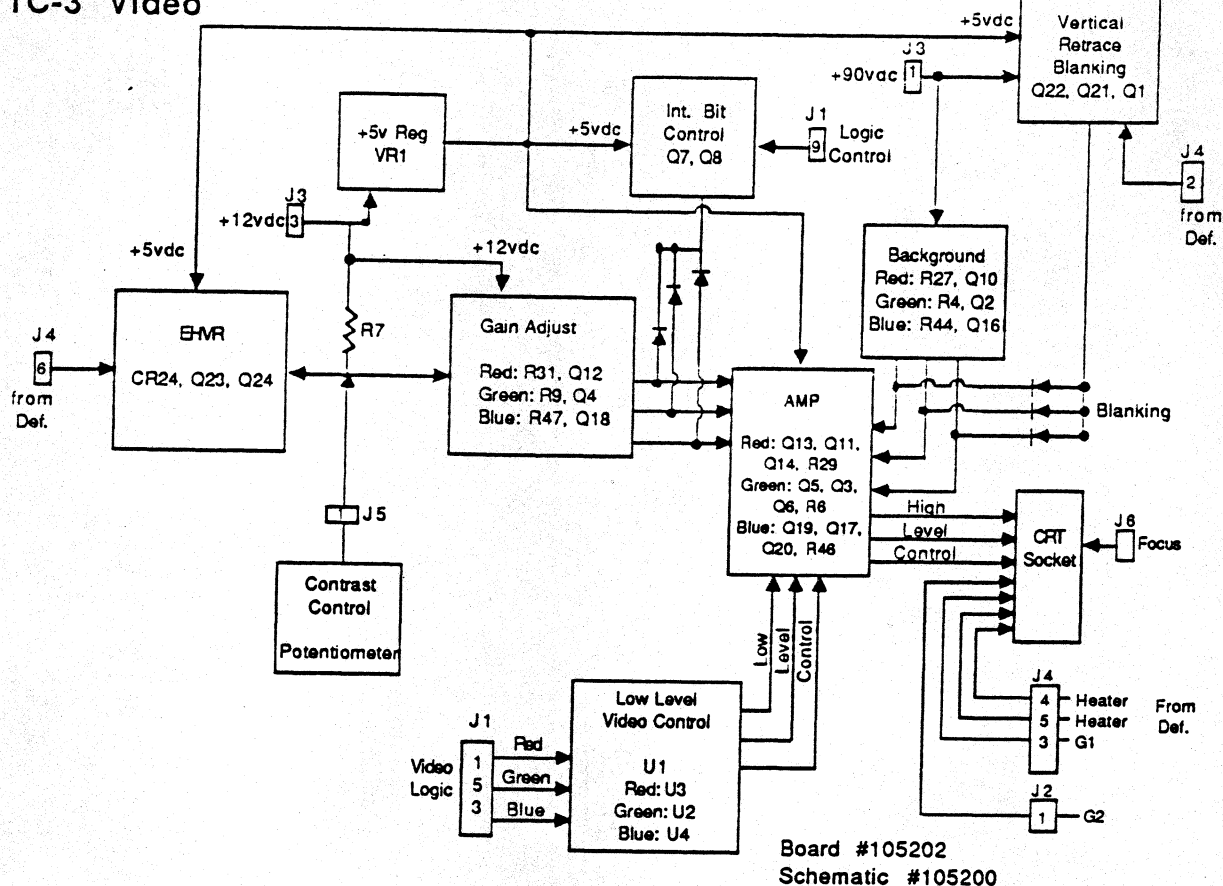
The TC-3 video amplifier board consists of three digital video driver channels. The amplifier channels are designed to accept one or two bit TTL digital input and provide drive to the CRT cathodes. Each amplifier has gain and bias adjustments to allow balancing of background and drive levels to the individual guns of the CRT.

Input and Output Wiring



BLOCK DIAGRAM

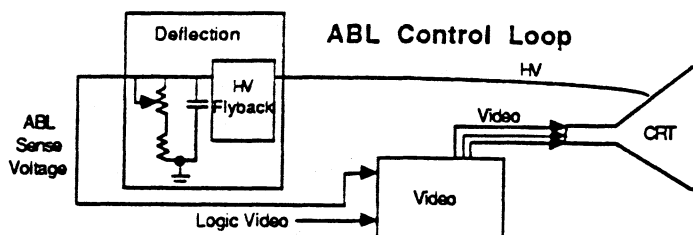
TC-3 Video



Circuit Description:

Video Gain Bus voltage through resistor R7 is used by the three **Gain Adjust** sections to set the gain of each amplifier. Any change in this voltage affects all three amplifiers simultaneously.

Automatic Beam Current Limiting (ABL), which is sometimes called Extended High Voltage Regulation (EHVR) circuitry automatically controls the gain of each amplifier section to limit the amount of current drawn by the cathodes of the CRT to a pre-set value. Circuitry consists of transistors Q23 and Q24, and diode CR24 with associated circuitry.



A current control loop is established by the ABL circuitry on the deflection and the video board.

Circuitry on the deflection board develops a negative voltage, input at J4, pin 6, that represents the current flowing through the high voltage flyback transformer. When the flyback current produces a voltage that exceeds about -7.5 VDC, zener diode CR24 starts to conduct and biases transistor Q24 on.

Q24 conducts and biases transistor Q23 on. The Video Gain Bus voltage is reduced when Q23 conducts. When the gain of the video amplifier is reduced, the cathode voltage is increased (screen intensity decreases) and current through the HV flyback transformer is reduced.

A voltage through resistor R66 charges capacitor C15 and biases Q24 off when the current through the flyback does not exceed the set limit.

C15 slows the response of the ABL circuitry to allow short duration, high peak, beam currents to occur. C15 also eliminates oscillation of the ABL system.

Contrast Control circuitry provides an external control of the Video Gain Bus voltage. An external 1K potentiometer is connected at J5, pins 1 and 2, in parallel with the output of the ABL circuitry.

Resistors R7, and R62, and the external contrast potentiometer form a voltage divider which controls the Video Gain Bus voltage.

Intensity Bit circuitry provides a way to modulate the output of all three video amplifiers simultaneously. The Logic board in 3800 and 8800 Series terminals does not generate an Intensity Bit. However, if the Intensity Bit circuitry fails, problems may develop in the amplifier and circuit description will be discussed. Transistors Q7 and Q8, diodes CR7, CR6, CR14, and CR20 are parts of this section.

A "low" input to J1, pin 9 biases Q7 on, which puts a positive voltage on the base of transistor Q8. When Q8 conducts, CR7, CR14, and CR20 are forward biased and the base bias voltage of the first stage amplifier in each Control Amplifier section is reduced at the same time.

Vertical Retrace Blanking circuitry simultaneously shuts off, or "Blanks", the output of all three video amplifiers during vertical retrace. Circuitry consists of transistors Q1, Q21, and Q22, diodes CR21, CR8, CR26, CR25, CR23, and CR22, and associated circuitry.

A positive TTL pulse is generated in the AR-2 deflection circuitry for every vertical retrace and input to the video board at J4, pin 2. Diode CR21 limits the input to +5 VDC.

Transistor Q1 is in parallel with each background circuit and is biased off by +90 VDC through resistor R41 when transistor Q21 is off.

The collector of transistor Q22 is tied to +5 VDC. During each vertical retrace pulse, Q22 conducts and biases Q21 on. When Q21 conducts, the base of Q1 is pulled toward ground and Q1 is biased on. Q1 bypasses each background circuit through diodes CR25, CR23, and CR22 and increases the base bias voltage to the second stage of the **Amplifier Control** circuitry.

Raising the voltage at this point effectively reduces the forward bias on each cathode of the CRT (cathode voltage is increased, display intensity decreased). Refer to the **Amplifier Control** section circuit description below to see how this is done.

Since the three video amplifier circuits are identical, only the Red channel is described below. Corresponding components, in the Green and Blue circuitry, perform identical functions.

Low Level Video Drive circuits provide digital to analog conversion and (when processing one bit video), act as an "on/off" switch for the **Amplifier Control** section. Integrated circuits U1, and U3 with associated circuitry, provide this function.

Low true TTL video logic is input to J1, pin 1. Jumper W1 should be installed to process the one bit video information from Intecolor 8800 series logic. A 74S04 buffer IC, U1, inverts the input and protects the logic from damaging noise spikes that may be present in the video amplifier circuitry.

When ground, or a "low", is applied to the inputs of U1, its outputs go "high". NAND gate U3, a 74S38 IC, inverts the signal from U1 and provides a low impedance path for current to flow from ground to the first stage amplifier of the **Amplifier Control** section. If the input to U1 goes "high" or opens, its output pins go low and U3 removes the path for current flow.

Resistors R36, R34, and R37 provide "weighting" of the current path from ground when the board is used for "two bit" video processing. Jumper W5 (position A for rev 1 boards or B for rev 2 boards), "tailors" the video output for different products. These resistor values were selected to make the video output colors match industry standards.

Schottky ICs are used to provide the fast turn-on and turn-off necessary to achieve the sharp rise and fall times at the output of the amplifier.

Gain Adjust circuitry sets the gain of the video amplifier. Transistor Q12, potentiometer R31, and associated circuitry provide this function.

The Video Gain Bus voltage from R7 is adjusted, by potentiometer R31, to control the bias of transistor Q12. Q12 buffers gain control R31, to provide a low impedance voltage source for base bias of transistor Q13, the first stage amplifier of the Amplifier Control section.

Diode CR14 prevents the bias voltage of the red amplifier stage from affecting any other stage.

The output of the gain adjust is a positive voltage on the base of transistor Q13.

Background circuitry provides an adjustable base bias voltage for the second stage amplifier in the Amplifier Control section. This circuitry is used to bias the cathodes of the CRT to just below conduction. Circuitry consists of transistor Q10, diode CR9, potentiometer R27, and associated circuitry.

Transistor Q10 collector is tied to +90 VDC, potentiometer R27 sets the bias on the base of Q10. Resistor R26 limits the bias of Q10 and insures that the output of the Vertical Retrace Blanking circuitry is a minimum of +10 VDC greater than the output of the Background circuitry.

Diodes CR9 and CR23 prevent the output of the red background circuitry from affecting the other two background circuits through the Vertical Retrace circuitry.

Amplifier Control circuitry provides amplification of the Low Level Video Drive signal, impedance matching to the CRT and buffers the low voltage circuitry from the CRT. Components in the Amplifier Control section are transistors Q13, Q11, and Q14, inductors L3 and L4, diodes CR10, CR11 and CR12, resistor R29 and associated components.

Video amplification is provided by a two stage amplifier. The first stage is common base amplifier, transistor Q13, and the second stage is a "push-pull" amplifier, complementary transistors Q11 and Q14.

The base of Q13 is biased to some positive DC voltage by the **Gain Adjust** circuits. Current flow for Q13 is from ground through the resistor R24, or the **Low Level Video Drive** circuits, Q13, diodes CR12, and CR11, inductor L3 and resistor R129 to the **Background** and **ABL** circuits.

Q11 and Q14 form a push-pull amplifier to drive the cathodes of the CRT. Current flow through the push-pull amplifier is from ground; through resistor R40, Q14, resistors R39 and R38, Q11, and resistor R30 to the +90 VDC provided by the power supply board. The output voltage to the cathode of the CRT is from common point of R39 and R38 through inductor L4.

Base bias voltage of Q11 and Q14 is controlled by the current flow through Q13. Diodes CR11 and CR12 each provide one diode voltage drop to compensate for voltage drops of Q11 and Q14 and insures that the "push-pull" transition of the amplifier is linear.

With no "Red" video enable, resistor R24 allows some current to flow from ground, through Q13, to the positive voltage from the **Background** circuits.

Increasing the **Background** voltage to Q13 increases the bias of Q11 and reduces the bias of Q14. The output voltage to the cathode of the CRT goes more positive and the display intensity decreases.

When the "Red" video is enabled, the low impedance path to ground, provided by U3, causes Q13 to increase conduction and its collector voltage drops. Base bias of Q11 is reduced and base bias of Q14 is increased. The output voltage of the amplifier decreases by about 50 volts and the CRT cathode is biased on.

Diode CR10 shunts high positive pulses that may be generated by CRT arcs to the +90 VDC supply. Diode CR13 shunts pulses more positive than +5 VDC to the +5 volt regulator to protect U3.

Inductor L3 peaks the collector circuit of Q13 for sharp rise and fall times. Inductor L4 resonates with the CRT capacitive load to provide improved rise and fall time at the CRT. Resistor R29 must be an Allen Bradley type to assure proper tube arc protection characteristics.

APPENDICES

APPENDIX A

3800/8800 PRODUCT LINE CHART

	CRT		Enclosure				Logic		Analog	
	19"	15"	Rack	Ergo	OEM	NEMA-2	Standard	Extended	Modular	Old Style
3810		X		X			X			X
3815		X		X			X		X	
3820		X		X				X		X
3825		X		X				X	X	
3860		X	X				X			X
3865		X	X				X		X	
3875		X	X					X	X	
8810	X			X			X			X
8814	X				X		X		X	
8815	X			X			X		X	
8816	X					X	X		X	
8820	X			X				X		X
8824	X				X			X	X	
8825	X							X	X	
8826	X					X		X	X	
8865	X		X				X		X	
8875	X		X					X	X	

APPENDIX B

FIRMWARE UPGRADE

Modifying 8800/3800 logic cards for V2.00 Firmware.

The modifications required for upgrading to V2.00 firmware for 8800/3800 Series Terminals can be accomplished on the logic assemblies 105150 and 105666 (PCB# 105149). The assemblies requiring hardware modification are based on the PCB# 105149, Rev. 1, 2, 2A and 2B. The PCB number and revision can be found in the "foil" on the back side of the logic card near the keyboard connector. Earlier logic cards (PCB# 102506) cannot be upgraded.

The modifications are listed below by revision level of the logic board.

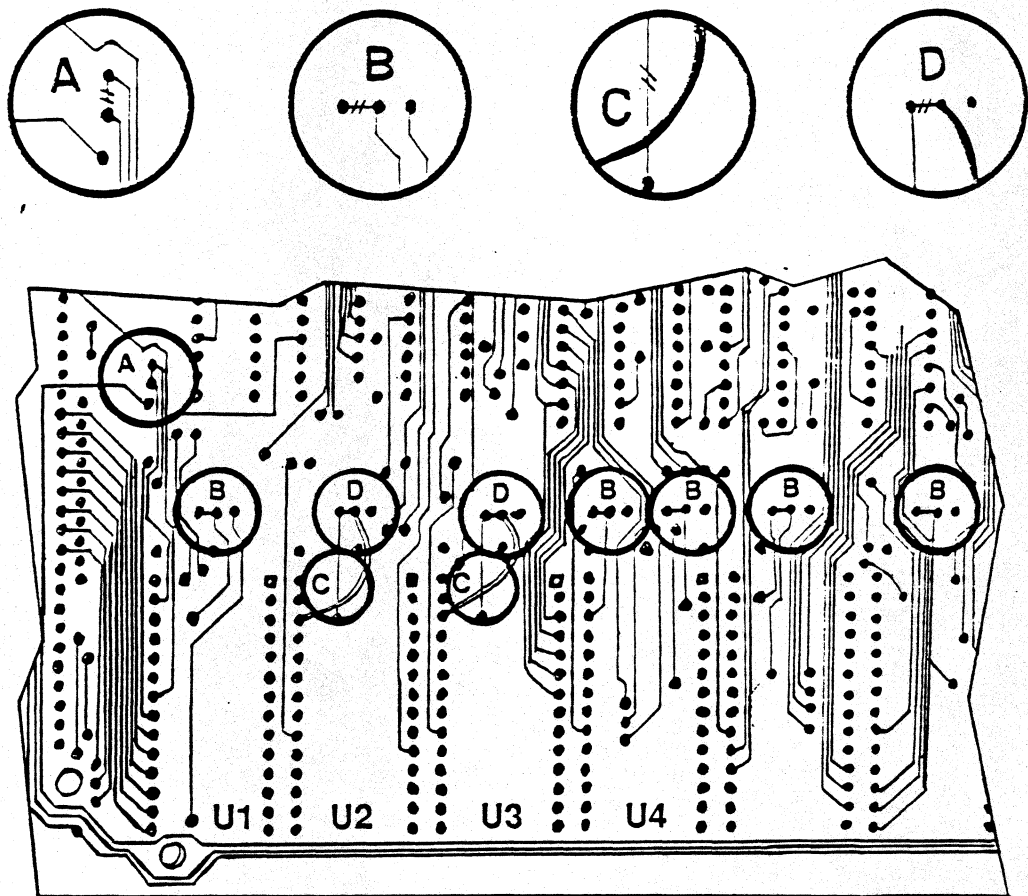
PCB# 105149, Rev. 3 and later

- a) Remove old firmware (U1-U4) and install new firmware.
- b) Replace the decoder in socket U20 (108032-040) with the new decoder 108100-200.
- c) Set the jumpers W3/W4, W5/W6, W7/W8 and W9/W10 for the 27256 EPROM (27128 and 27256 EPROMs use the same setting). See label on logic board.
- d) Set the jumper W11/W12 for an EPROM at U4.
- e) Set the jumper W40/W41 for the 27256 EPROM (W41 setting).

PCB# 105149, Rev. 2, 2A, 2b

- a) Remove old firmware (U1-U4) and install new firmware.
- b) Replace the decoder in socket U20 (108032-040) with the new decoder 108100-200.
- c) Cut jumper defaults on jumpers W3/W4, W5/W6, W7/W8, W9/W10 and W11/W12 (see figure, details B and D). Install three-pin headers with shorting plugs ("suitcases").
- d) Set the jumpers W3/W4, W5/W6, W7/W8 and W9/W10 for the 27256 EPROM (27128 and 27256 EPROMs use the same settings).
- e) Set the jumper W11/W12 for an EPROM at U4.
- f) Cut the trace that runs from the W6 side of the W5/W6 jumper toward socket U2 (see figure, detail C) and install jumper from pin 26 of U2 to the center pin of jumper W5/W6 (see figure, detail D).
- g) Cut the trace that runs from the W8 side of the W7/W8 jumper toward socket U3 (see figure, detail C) and install jumper from pin 26 of U3 to the center pin of jumper W7/W8 (see figure, detail D.)

- h) Cut the jumper default on jumper W40/W41 (see figure, detail A) and install a three-pin header with shorting plug ("suitcase").
- i) Set the jumper W40/W41 for the 27256 EPROM (W41 setting).
- j) For 8810/3810/3860 terminals also do the following:
 - 1) Cut the jumper defaults on jumpers W13/W14 and W15/W16 (see figure, detail B). Install three-pin headers with shorting plugs ("suitcase").
 - 2) Remove the 2Kx8 RAM from U5 and install two 8Kx8 Ram chips in sockets U5 and U6.



// represents cutting a jumper/trace

- a) Remove old firmware (U1-U4) and install new firmware.
- b) Replace the decoder in socket U20 (108032-040) with the new decoder 108100-200.
- c) Cut jumper defaults on W3/W4, W5/W6, W7/W8, W9/W10 and W11/W12 (see figure, details B and D). Install three-pin headers with shorting plugs ("suitcase").
- d) Set the jumpers W3/W4, W5/W6, W7/W8, and W9/W10 for the 27256 EPROM (27128 and 27256 EPROMs use the same setting).
- e) Set the jumper W11/W12 for an EPROM at U4.
- f) Cut the trace that runs from the W6 side of W5/W6 jumper toward socket U2 (see figure, detail C) and install jumper from pin 26 of U2 to the center pin of jumper W5/W6 (see figure, detail D).
- g) Cut the trace that runs from the W8 side of the W7/W8 jumper toward socket U3 (see figure, detail C) and install jumper from pin 26 of U3 to the center pin of jumper W7/W8 (see figure, detail D).
- h) Cut the jumper default on jumper W40/W41 (see figure, detail A) and install a three-pin header with a shorting plug ("suitcase").
- i) Set the jumper W40/W41 for the 27256 EPROM (W41 setting).
- j) For 8810/3810/3860 terminals also do the following:
 - 1) Cut the jumper defaults on jumpers W13/W14 and W15/W16 (see figure, detail B). Install three-pin headers with shorting plugs ("suitcase").
 - 2) Remove the 2Kx8 RAM from U5 and install two 8Kx8 Ram chips in sockets U5 and U6.
- k) If the light pen is to be used with assembly and it was not previously installed, other modifications may be required; consult factory.

After installing the new firmware, power the unit on and wait until it successfully completes the selftest (Tone sounds and power up message appears) or it displays the Setup menu. In the Setup menu set the appropriate parameters (defaults are suggested), save these and exit. In V2.00 firmware, there are two main menus (Host I/O and Operator Preference) and the Hardware Configuration menu.

If there are questions or comments, please call Intecolor Technical Support at (404) 449-5961.

APPENDIX C COVER REMOVAL

Power should always be removed before servicing a unit.

A #2 Phillips screwdriver is required for cover removal.

WARNING! Do not apply power to the unit with circuit boards hanging from the chassis by connecting cables and cords. Electrical shock and/or damage to the unit could result. The inside of the covers are painted with a conductive coating.

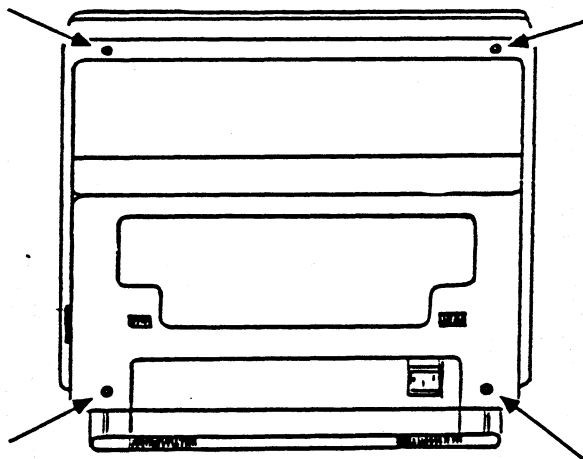
WARNING! Any maintenance performed with power on and cover off subjects the operator to electrical shock hazards that could cause injury or death. Such maintenance should be performed by trained and qualified service personnel who are aware of the existing hazards.

The 3815, and 3825 terminals use the same cover as the 3810.

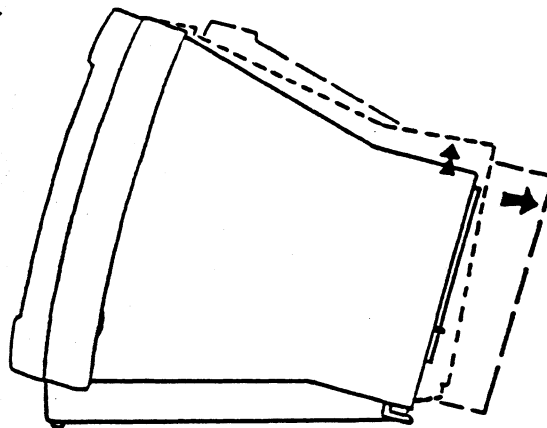
First, remove the two Phillips head screws at the top rear of CRT bezel.

Second, remove the two Phillips head screws at the rear bottom of cabinet.

Third, lift the rear of the cover up, then slide the cover to the rear and off the unit.



1st - remove phillips screws

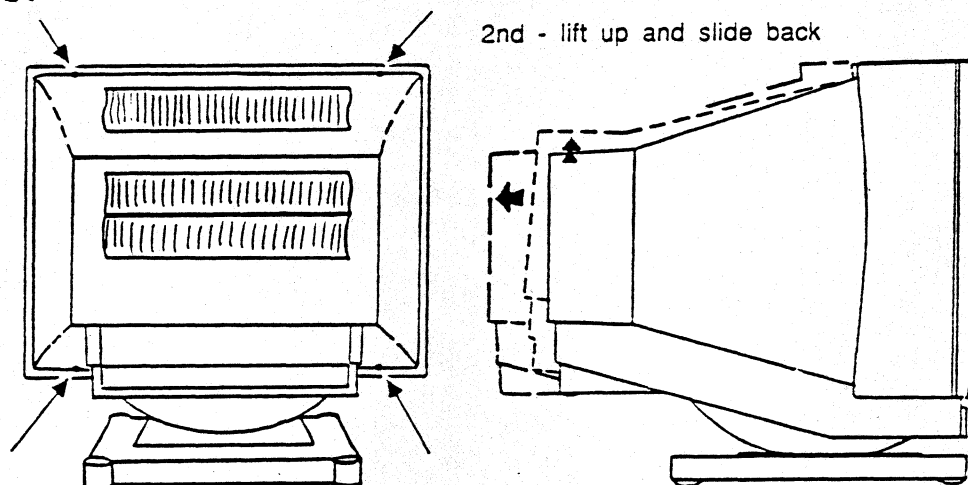


2nd - lift up and slide back

The 8815 and 8825 cover may be removed following the instructions below.

First, remove the four Phillips screws at the top and bottom rear of the CRT bezel.

Second, carefully slide the cover toward the rear and off the chassis.



1st - remove phillips screws from rear

Rack-mount unit cover removal is described below.

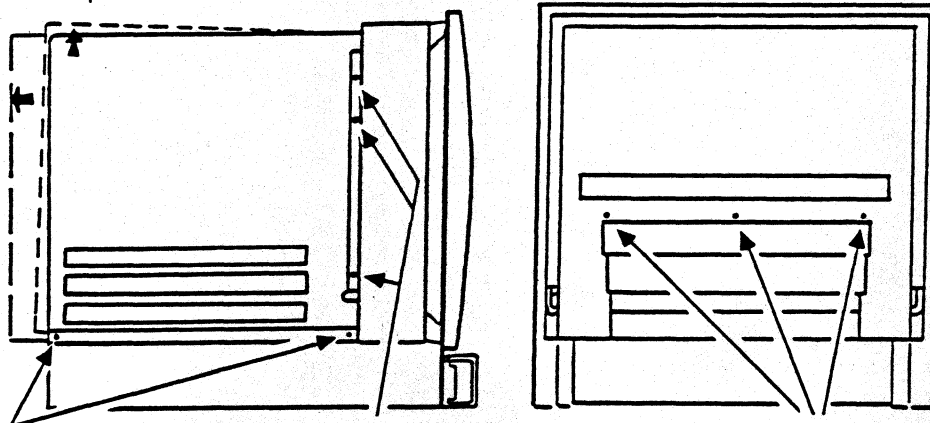
First, remove the three Phillips head screws down the front of each side of the metal cover. (6 screws total)

Second, remove the two Phillips head screws along the bottom of each side of the metal cover. (4 screws total)

Third, remove the three Phillips screws above the I/O port plate on the rear of the metal cover.

Fourth, carefully slide the metal cover to the rear and off the unit.

4th - lift up and slide back



2nd - remove phillips screws (each side of unit)

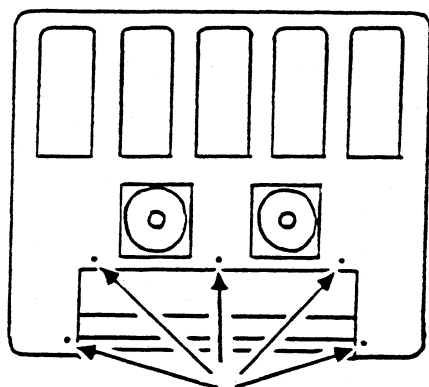
1st - remove phillips screws (each side of unit)

3rd - remove phillips screws from rear

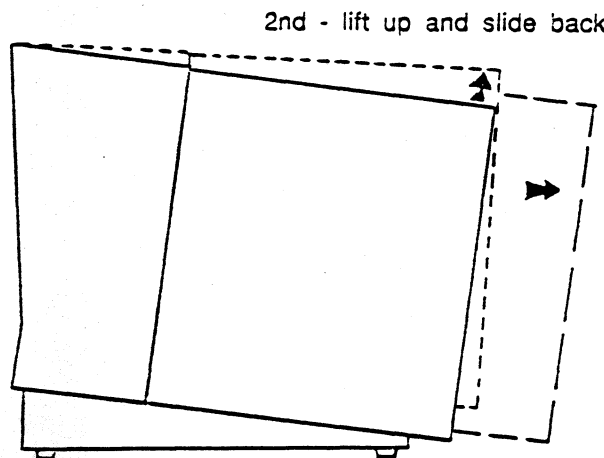
NEMA-2 enclosure removal is described below.

First, remove the five Phillips head screws fastening the cover to the rear connector panel (three along the top and one on each side of the connector panel).

Next, carefully slide the metal cover to the rear and off the unit.



1st - remove phillips screws



2nd - lift up and slide back

APPENDIX D CIRCUIT BOARD LAYOUT

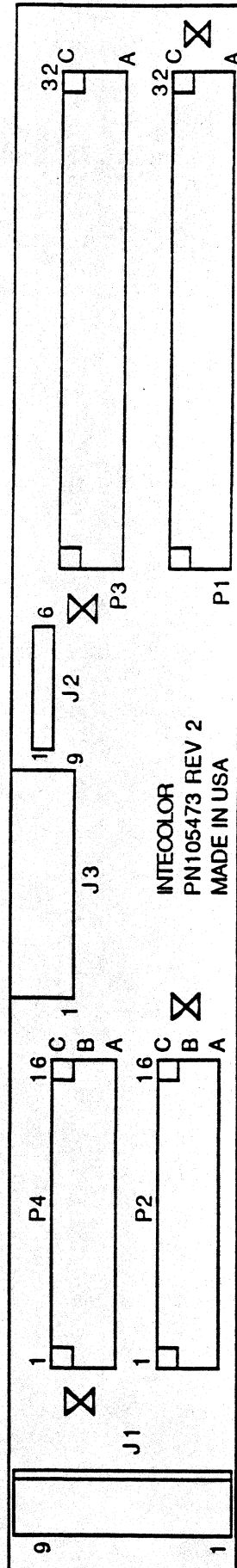
Printed Circuit Board (PCB) silkscreen drawings are provided for parts and test point location on the circuit assemblies.

The part number for each modular assembly is printed on a sticker which normally can be found on the component side of the PCB.

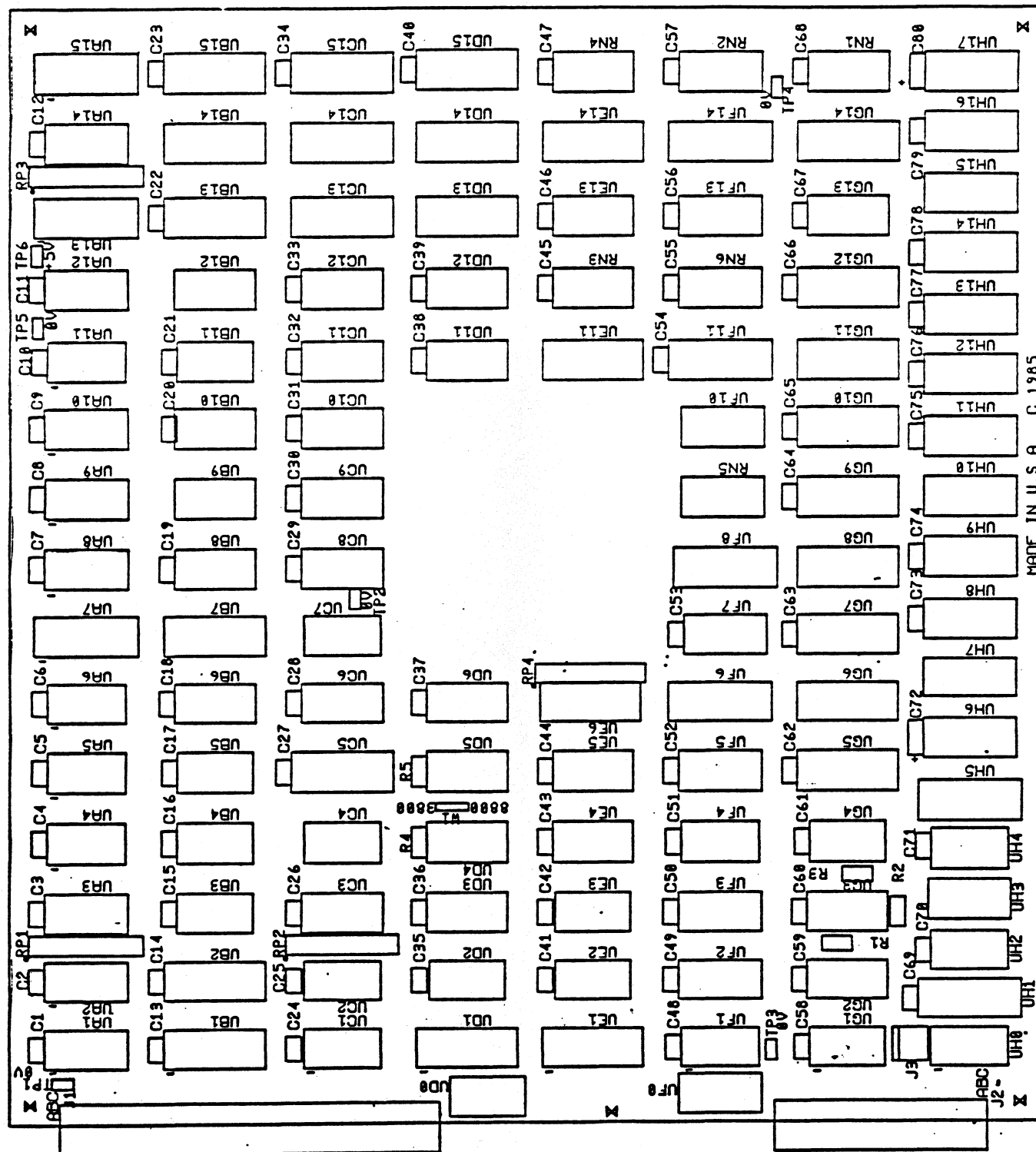
Only the assemblies described in this addendum are provided.

	ASSEMBLY#	PCB DRAWING#	Page#
Mother Board.....	105471.....	105473.....	D.2
Graphics Board.....	105194.....	102912 Rev.3.....	D.3
Extended Graphics.....	105408.....	102912 Rev 3.....	D.3
KM-3 Power Supply	105669.....	105668.....	D.4
KM-4 Power Supply	105766.....	105765.....	D.5
AR-2 Power Supply	105684.....	105683.....	D.6
KM-3 Deflection	103302.....	103301.....	D.7
KM-4 Deflection	105763.....	105762.....	D.8
AR-2 Deflection	105157.....	105156.....	D.9
TC-1 Video	105112.....	105111.....	D.10
TC-3 Video	105202.....	105201.....	D.11
AR-2 Video	105199.....	105198.....	D.12

PCB P/N 105473 REV-2 MOTHERBOARD



PCB P/N 102912 REV-3 GRAPHICS BOARD



MADE IN U.S.A. C 1985

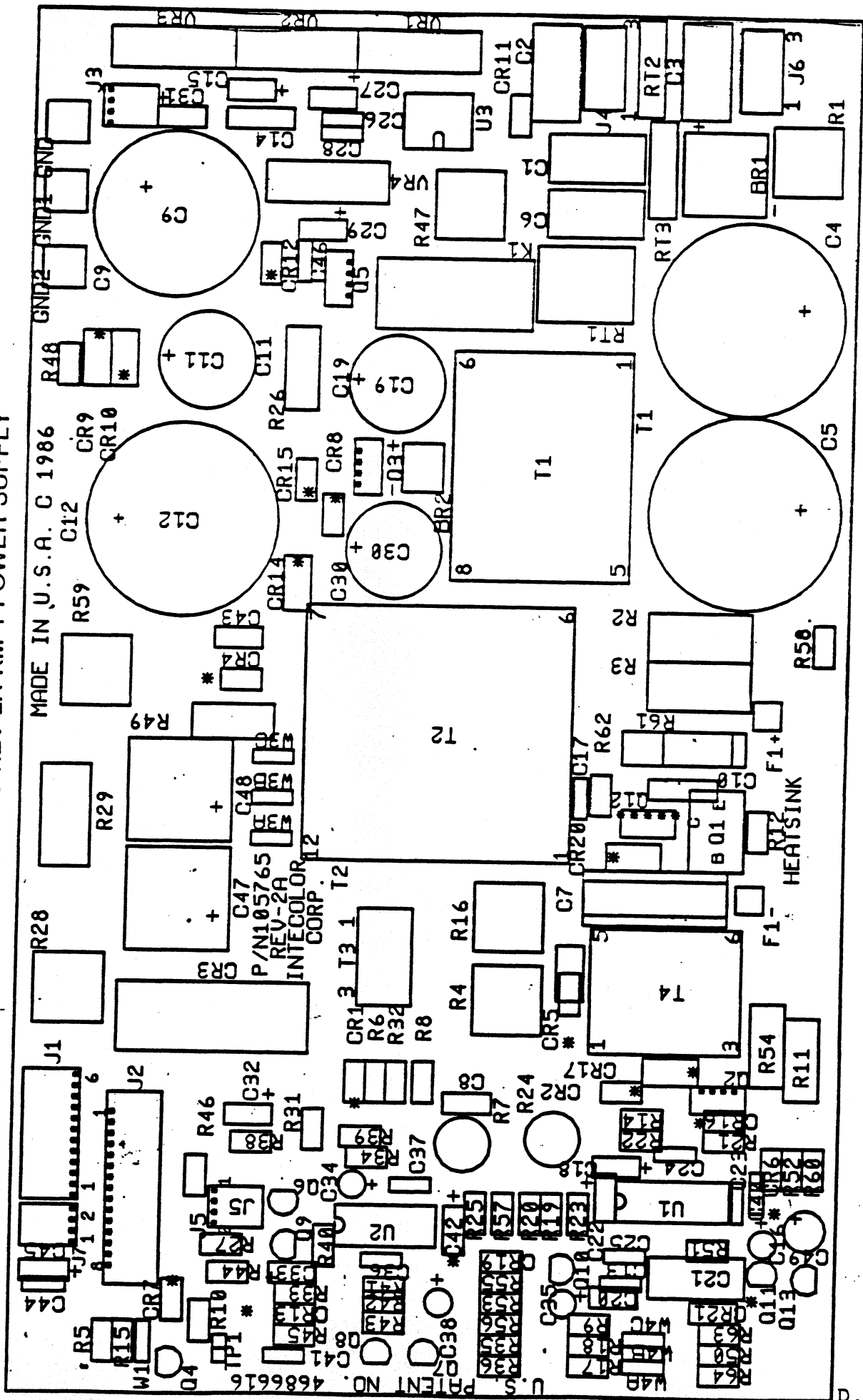
MADE IN U.S.A. C 1986

GND1

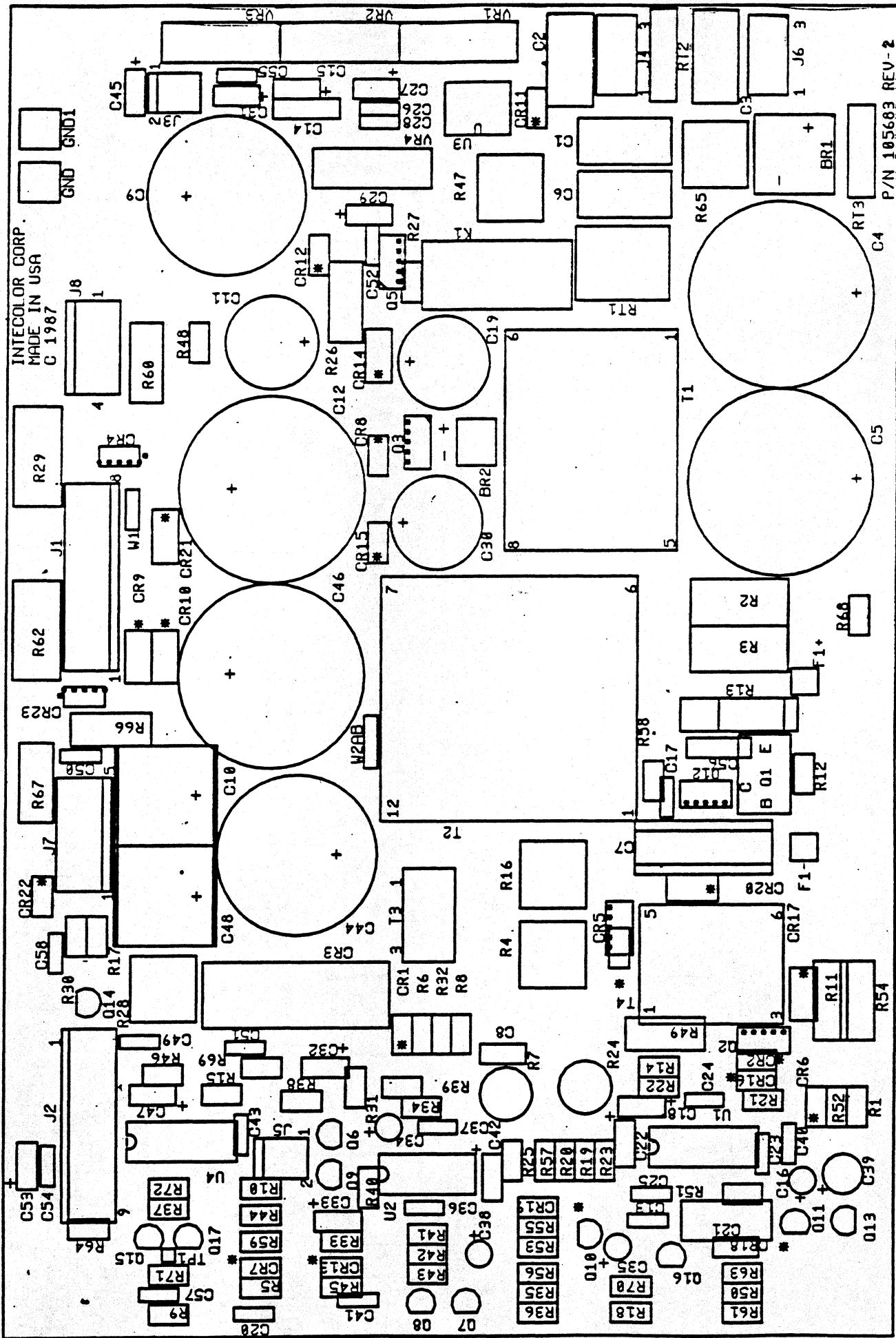
GND2

P/N 105668
REV-2

PCB P/N 105765 REV-2A KM-4 POWER SUPPLY



PCB P/N 105683 REV-2 AR-2 POWER SUPPLY

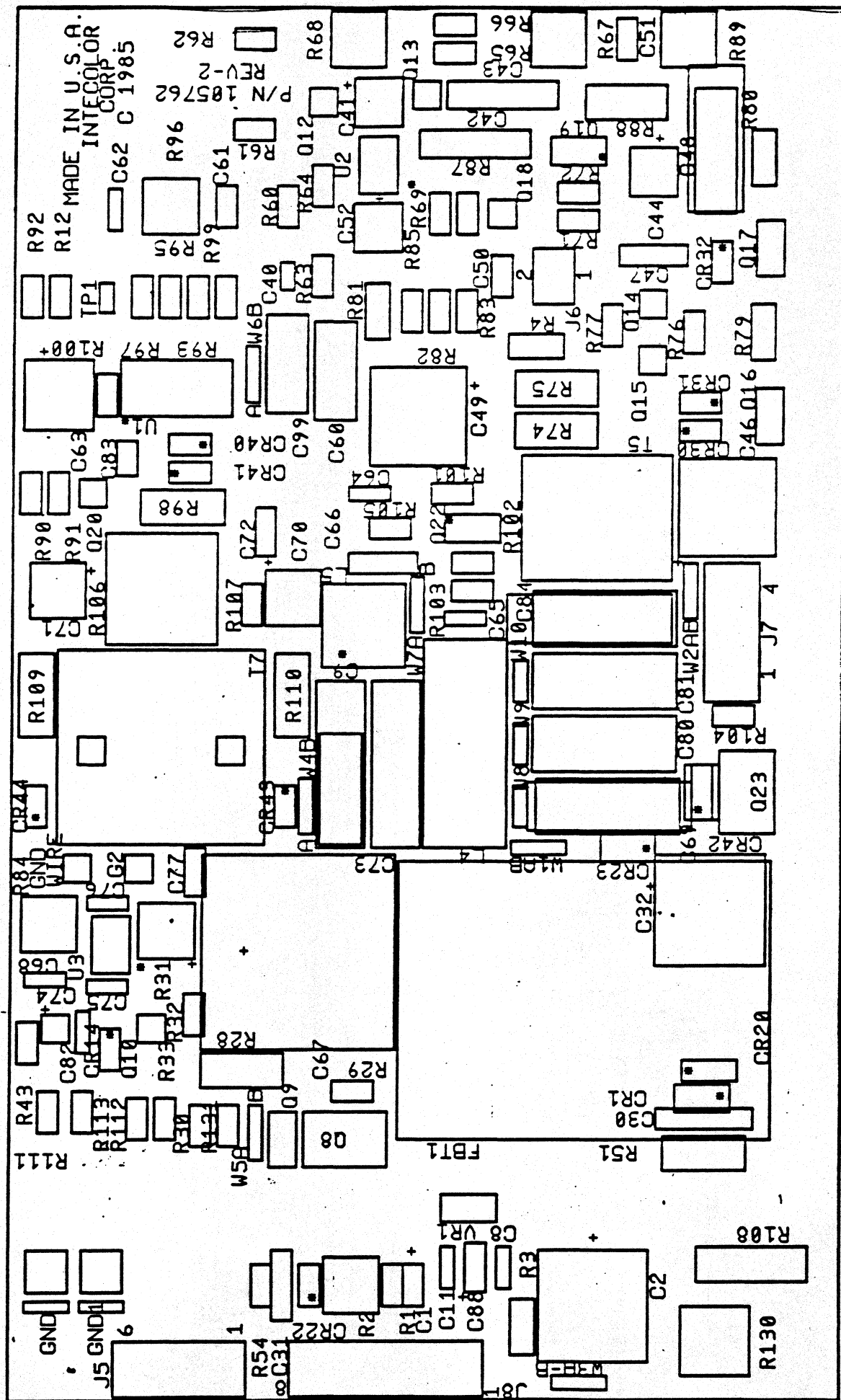


INTECOLOR CORP.
 MADE IN USA
 C 1987

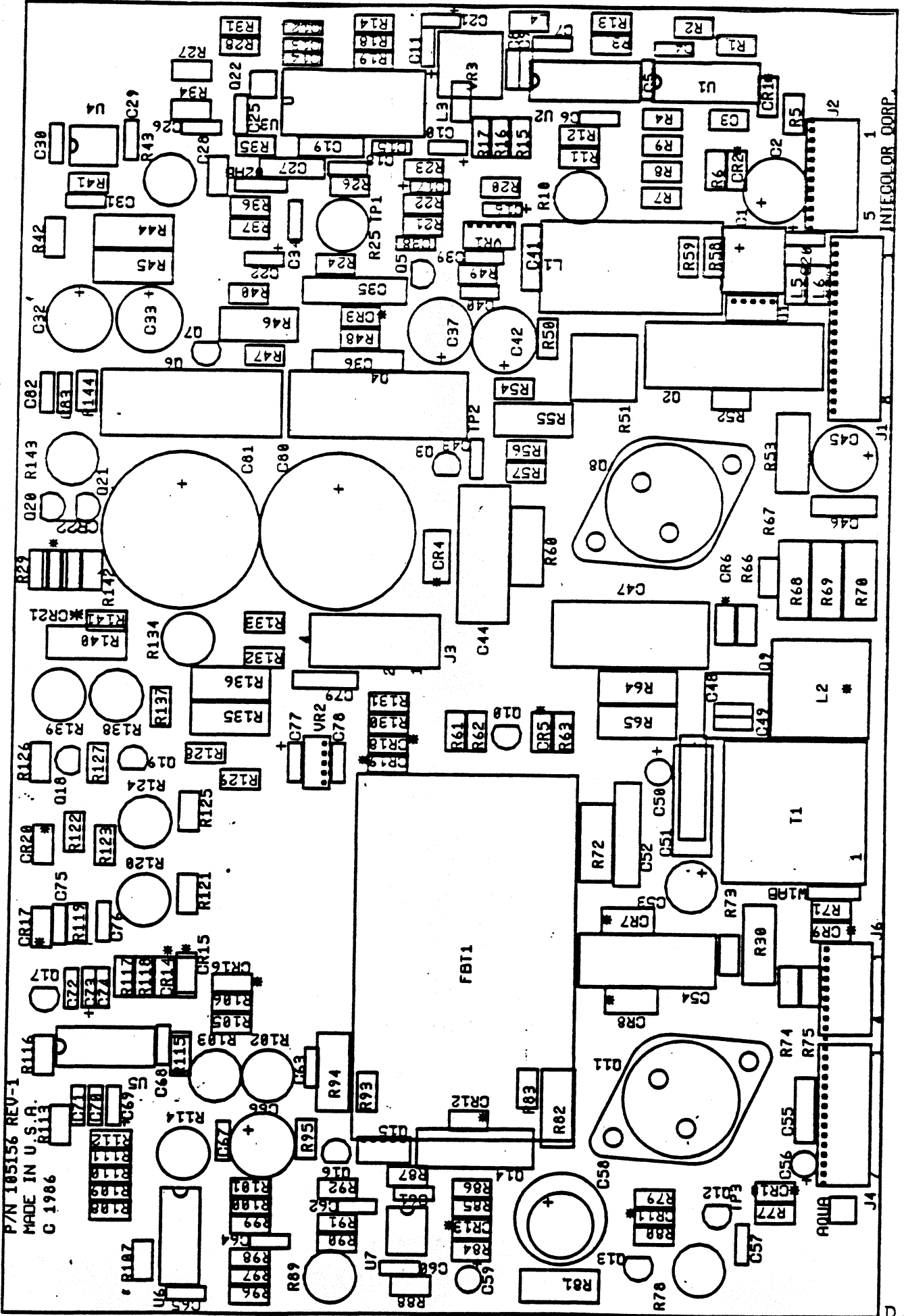
P/N 105683 REV-2

R111 R43 R49 R113 R112 R30 R33 R32 R31 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R145 R146 R147 R148 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174 R175 R176 R177 R178 R179 R180 R181 R182 R183 R184 R185 R186 R187 R188 R189 R190 R191 R192 R193 R194 R195 R196 R197 R198 R199 R200 R201 R202 R203 R204 R205 R206 R207 R208 R209 R210 R211 R212 R213 R214 R215 R216 R217 R218 R219 R220 R221 R222 R223 R224 R225 R226 R227 R228 R229 R230 R231 R232 R233 R234 R235 R236 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249 R250 R251 R252 R253 R254 R255 R256 R257 R258 R259 R260 R261 R262 R263 R264 R265 R266 R267 R268 R269 R270 R271 R272 R273 R274 R275 R276 R277 R278 R279 R280 R281 R282 R283 R284 R285 R286 R287 R288 R289 R290 R291 R292 R293 R294 R295 R296 R297 R298 R299 R300 R301 R302 R303 R304 R305 R306 R307 R308 R309 R310 R311 R312 R313 R314 R315 R316 R317 R318 R319 R320 R321 R322 R323 R324 R325 R326 R327 R328 R329 R330 R331 R332 R333 R334 R335 R336 R337 R338 R339 R340 R341 R342 R343 R344 R345 R346 R347 R348 R349 R350 R351 R352 R353 R354 R355 R356 R357 R358 R359 R360 R361 R362 R363 R364 R365 R366 R367 R368 R369 R370 R371 R372 R373 R374 R375 R376 R377 R378 R379 R380 R381 R382 R383 R384 R385 R386 R387 R388 R389 R390 R391 R392 R393 R394 R395 R396 R397 R398 R399 R400 R401 R402 R403 R404 R405 R406 R407 R408 R409 R410 R411 R412 R413 R414 R415 R416 R417 R418 R419 R420 R421 R422 R423 R424 R425 R426 R427 R428 R429 R430 R431 R432 R433 R434 R435 R436 R437 R438 R439 R440 R441 R442 R443 R444 R445 R446 R447 R448 R449 R450 R451 R452 R453 R454 R455 R456 R457 R458 R459 R460 R461 R462 R463 R464 R465 R466 R467 R468 R469 R470 R471 R472 R473 R474 R475 R476 R477 R478 R479 R480 R481 R482 R483 R484 R485 R486 R487 R488 R489 R490 R491 R492 R493 R494 R495 R496 R497 R498 R499 R500 R501 R502 R503 R504 R505 R506 R507 R508 R509 R510 R511 R512 R513 R514 R515 R516 R517 R518 R519 R520 R521 R522 R523 R524 R525 R526 R527 R528 R529 R530 R531 R532 R533 R534 R535 R536 R537 R538 R539 R540 R541 R542 R543 R544 R545 R546 R547 R548 R549 R550 R551 R552 R553 R554 R555 R556 R557 R558 R559 R560 R561 R562 R563 R564 R565 R566 R567 R568 R569 R570 R571 R572 R573 R574 R575 R576 R577 R578 R579 R580 R581 R582 R583 R584 R585 R586 R587 R588 R589 R590 R591 R592 R593 R594 R595 R596 R597 R598 R599 R600 R601 R602 R603 R604 R605 R606 R607 R608 R609 R610 R611 R612 R613 R614 R615 R616 R617 R618 R619 R620 R621 R622 R623 R624 R625 R626 R627 R628 R629 R630 R631 R632 R633 R634 R635 R636 R637 R638 R639 R640 R641 R642 R643 R644 R645 R646 R647 R648 R649 R650 R651 R652 R653 R654 R655 R656 R657 R658 R659 R660 R661 R662 R663 R664 R665 R666 R667 R668 R669 R670 R671 R672 R673 R674 R675 R676 R677 R678 R679 R680 R681 R682 R683 R684 R685 R686 R687 R688 R689 R690 R691 R692 R693 R694 R695 R696 R697 R698 R699 R700 R701 R702 R703 R704 R705 R706 R707 R708 R709 R710 R711 R712 R713 R714 R715 R716 R717 R718 R719 R720 R721 R722 R723 R724 R725 R726 R727 R728 R729 R730 R731 R732 R733 R734 R735 R736 R737 R738 R739 R740 R741 R742 R743 R744 R745 R746 R747 R748 R749 R750 R751 R752 R753 R754 R755 R756 R757 R758 R759 R760 R761 R762 R763 R764 R765 R766 R767 R768 R769 R770 R771 R772 R773 R774 R775 R776 R777 R778 R779 R780 R781 R782 R783 R784 R785 R786 R787 R788 R789 R790 R791 R792 R793 R794 R795 R796 R797 R798 R799 R800 R801 R802 R803 R804 R805 R806 R807 R808 R809 R810 R811 R812 R813 R814 R815 R816 R817 R818 R819 R820 R821 R822 R823 R824 R825 R826 R827 R828 R829 R830 R831 R832 R833 R834 R835 R836 R837 R838 R839 R840 R841 R842 R843 R844 R845 R846 R847 R848 R849 R850 R851 R852 R853 R854 R855 R856 R857 R858 R859 R860 R861 R862 R863 R864 R865 R866 R867 R868 R869 R870 R871 R872 R873 R874 R875 R876 R877 R878 R879 R880 R881 R882 R883 R884 R885 R886 R887 R888 R889 R890 R891 R892 R893 R894 R895 R896 R897 R898 R899 R900 R901 R902 R903 R904 R905 R906 R907 R908 R909 R910 R911 R912 R913 R914 R915 R916 R917 R918 R919 R920 R921 R922 R923 R924 R925 R926 R927 R928 R929 R930 R931 R932 R933 R934 R935 R936 R937 R938 R939 R940 R941 R942 R943 R944 R945 R946 R947 R948 R949 R950 R951 R952 R953 R954 R955 R956 R957 R958 R959 R960 R961 R962 R963 R964 R965 R966 R967 R968 R969 R970 R971 R972 R973 R974 R975 R976 R977 R978 R979 R980 R981 R982 R983 R984 R985 R986 R987 R988 R989 R990 R991 R992 R993 R994 R995 R996 R997 R998 R999 R1000

PCB P/N 105762 REV-2 KM4 DEFLECTION

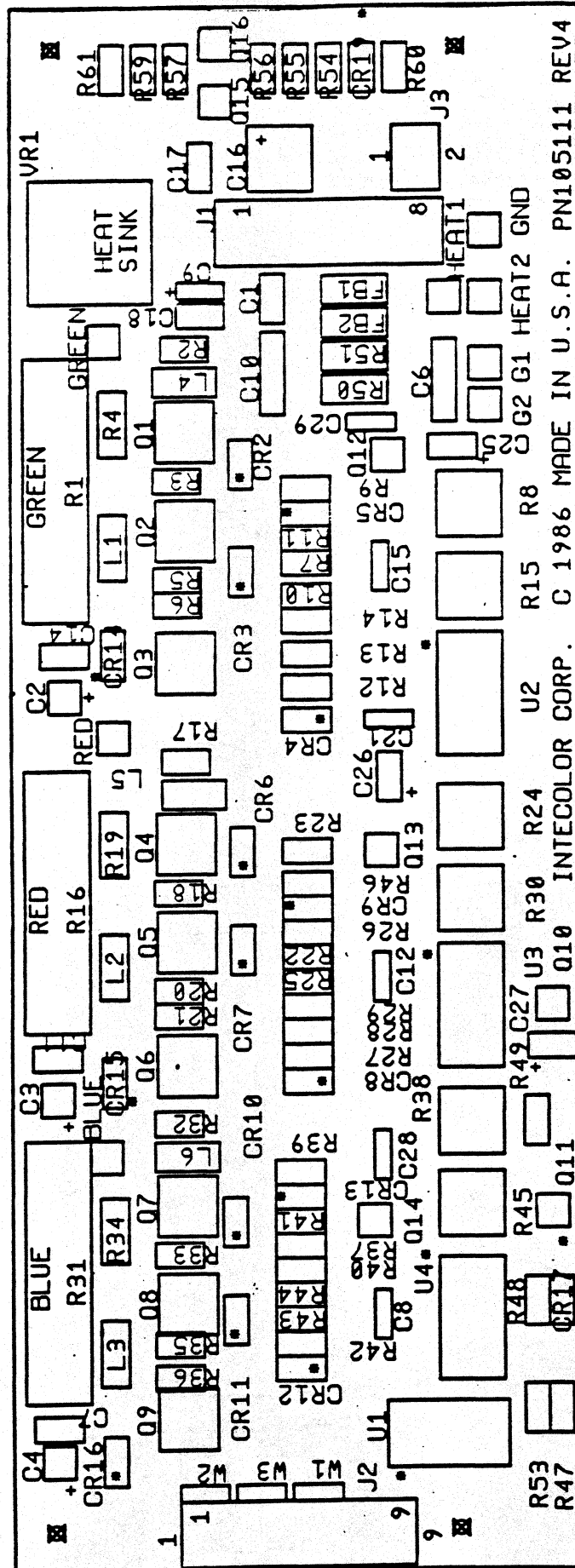


PCB P/N 105156 REV-1 R AR-2 DEFLECTION

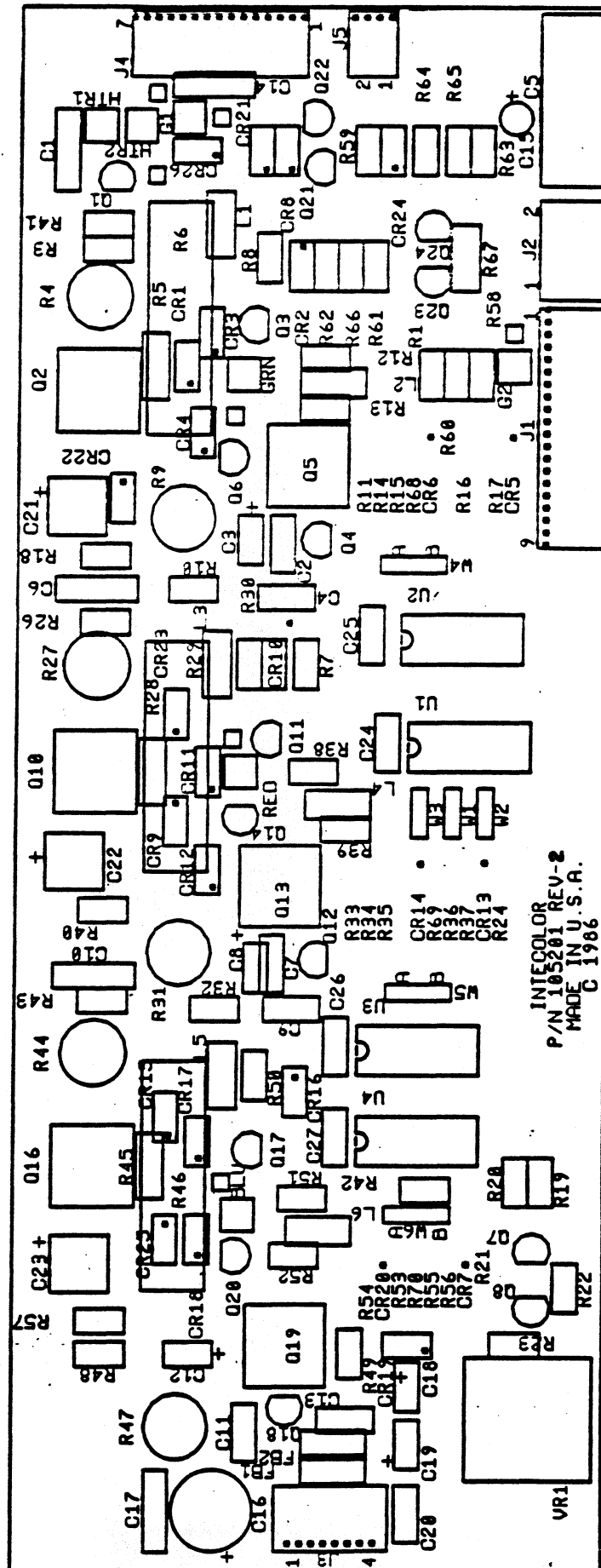


INTECOLOR CORP.

PCB P/N 105111 REV-4 TC-1 VIDEO

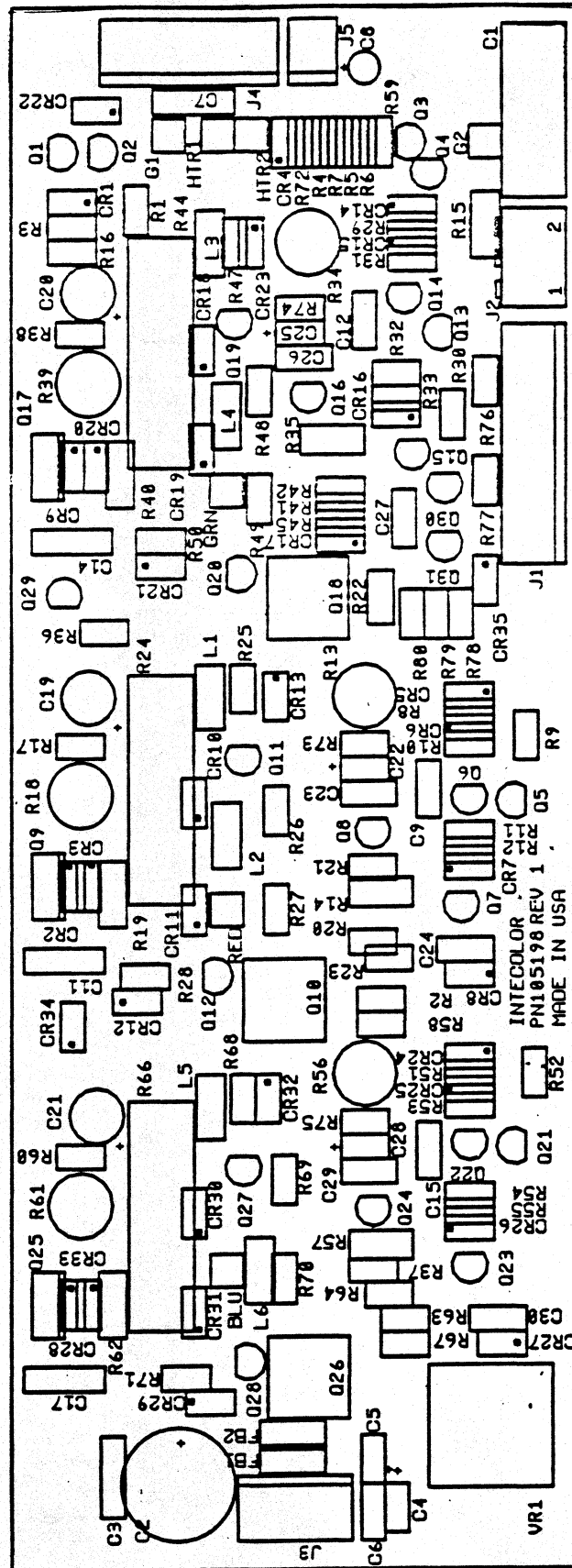


PCB P/N 105201 REV-2 TC-3 VIDEO



INTECOLOR
P/N 105201 REV-2
MADE IN U.S.A.
C 1986

PCB P/N 105198 REV-1 AR-2 VIDEO

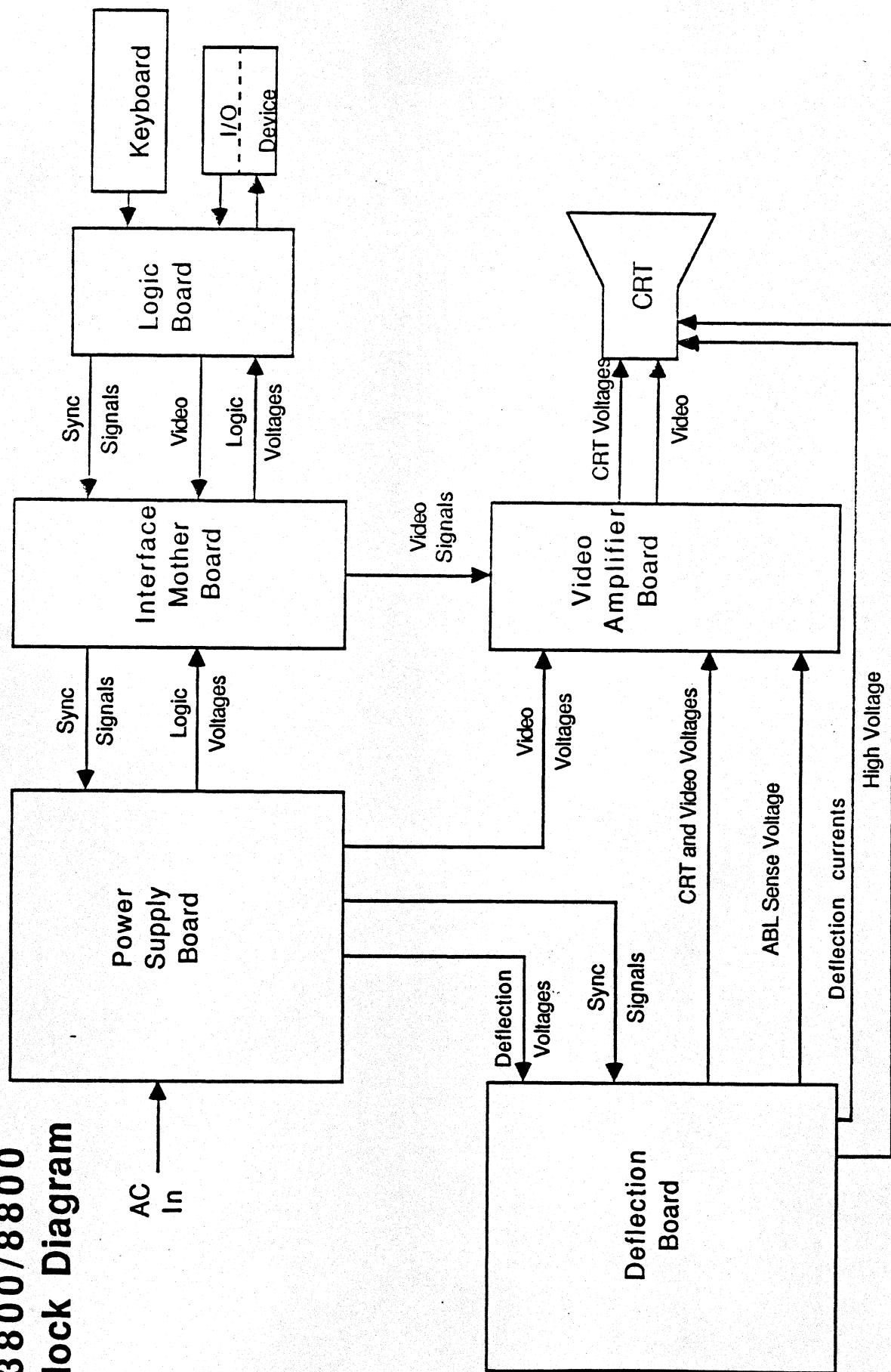


APPENDIX E ANALOG BOARD BLOCK DIAGRAMS

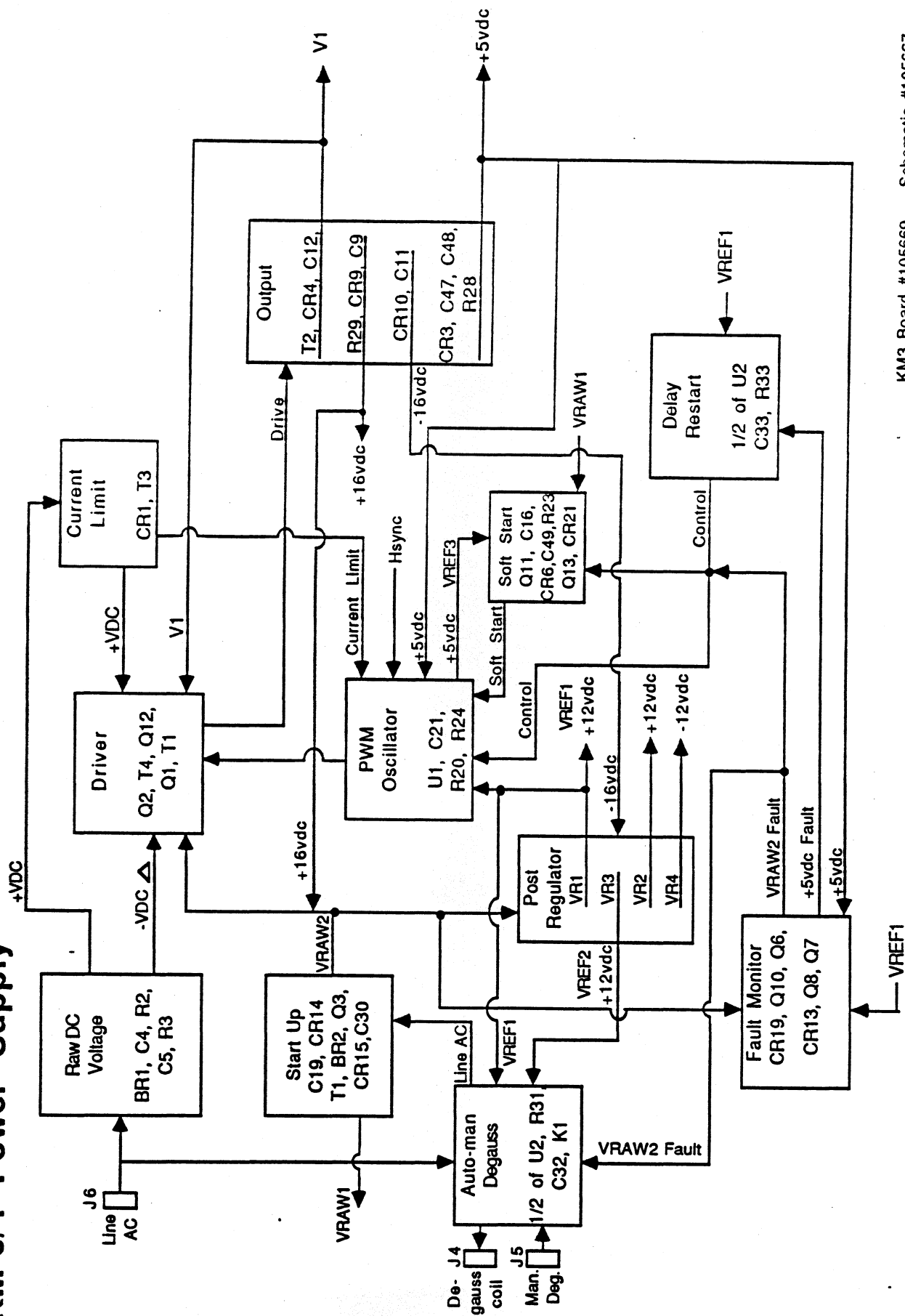
Block diagrams for each analog board described in the circuit description section of this addendum are provided.

SYSTEM	page E.2
KM-3 POWER SUPPLY	page E.3
KM-4 POWER SUPPLY	page E.3
AR-2 POWER SUPPLY	page E.4
KM-3 DEFLECTION	page E.5
KM-4 DEFLECTION	page E.5
AR-2 DEFLECTION	page E.6
TC-1 VIDEO	page E.7
TC-3 VIDEO	page E.8
AR-2 VIDEO	page E.9

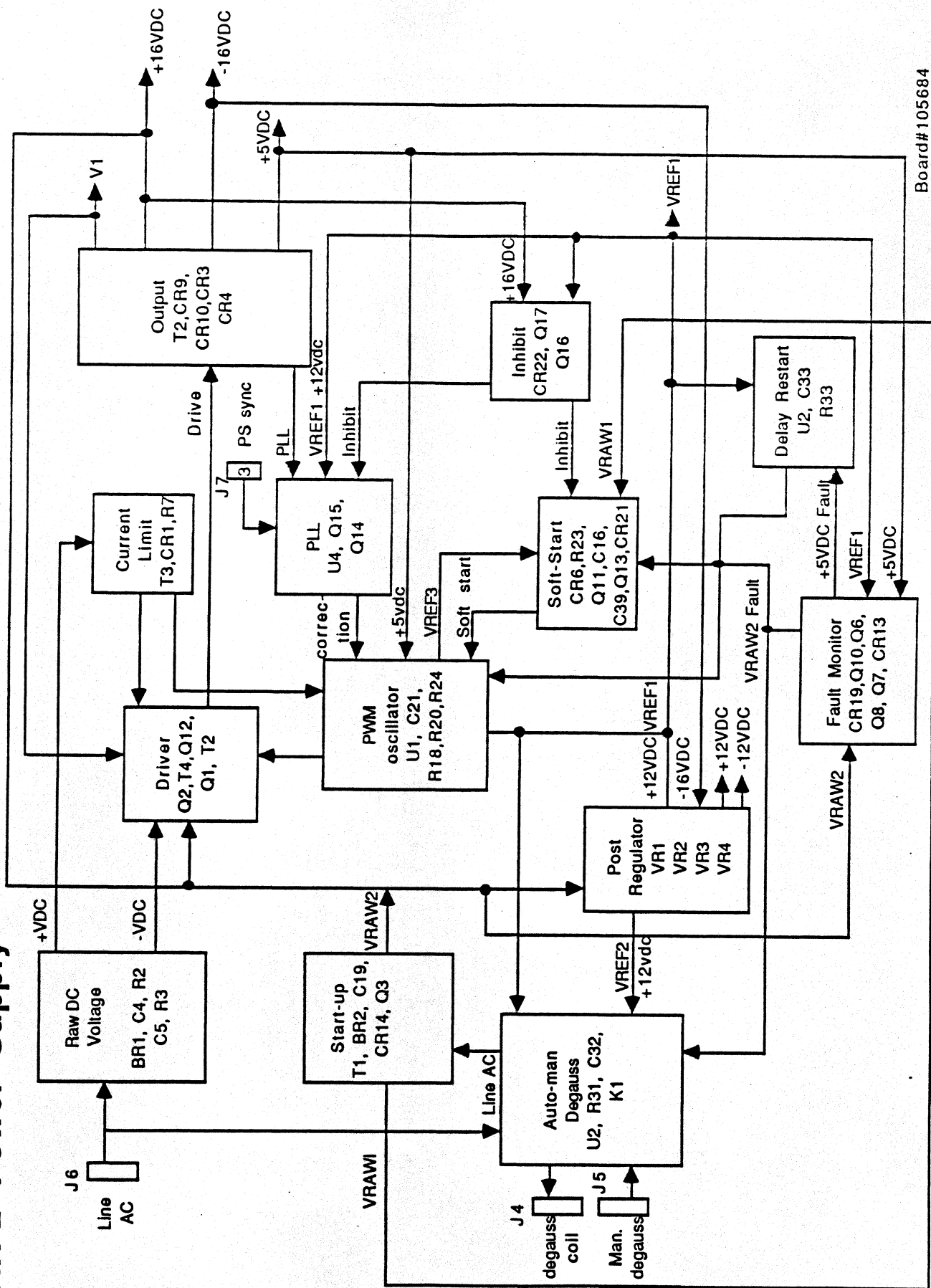
3800/8800 Block Diagram



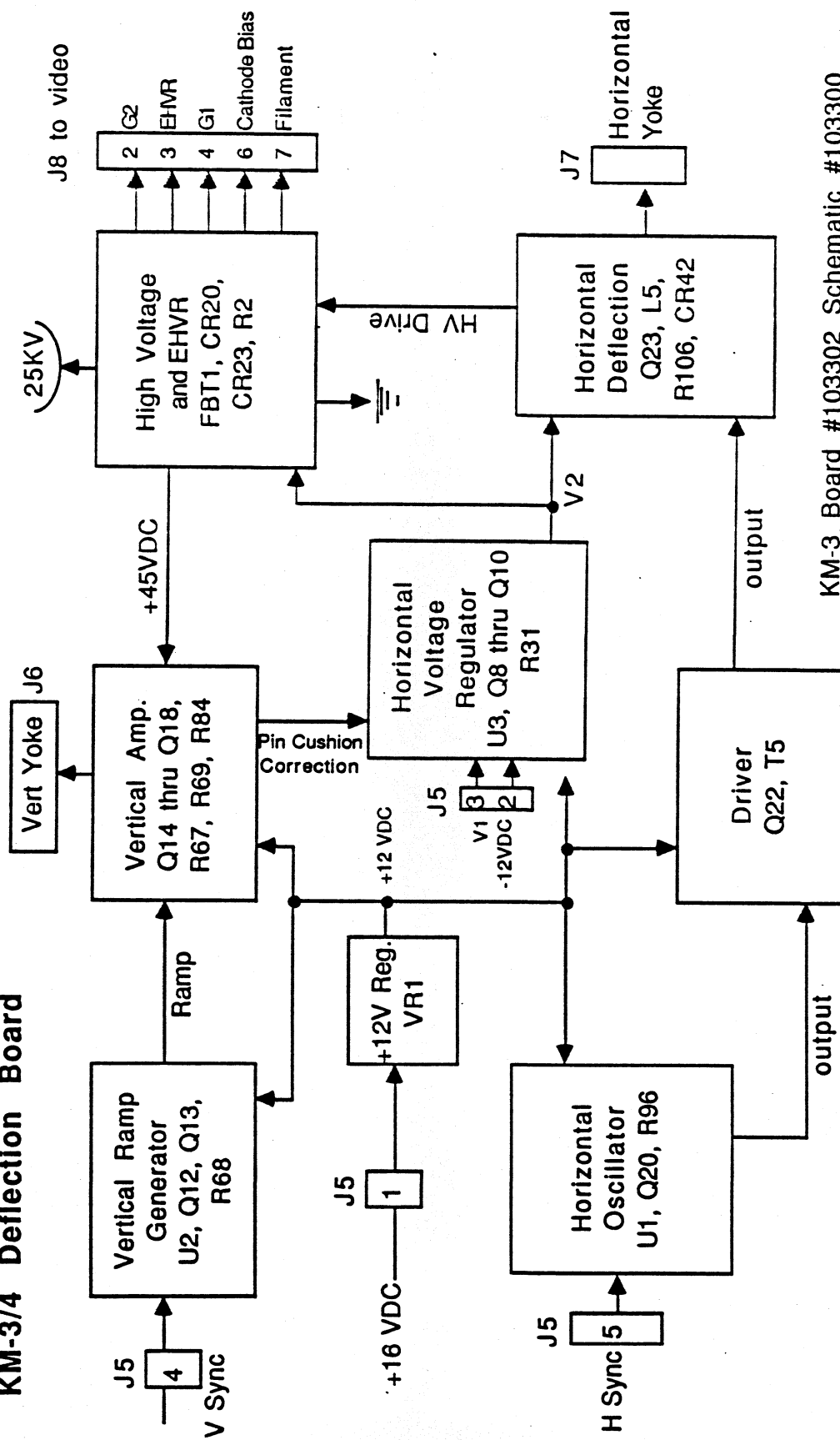
KM-3/4 Power Supply



AR-2 Power Supply

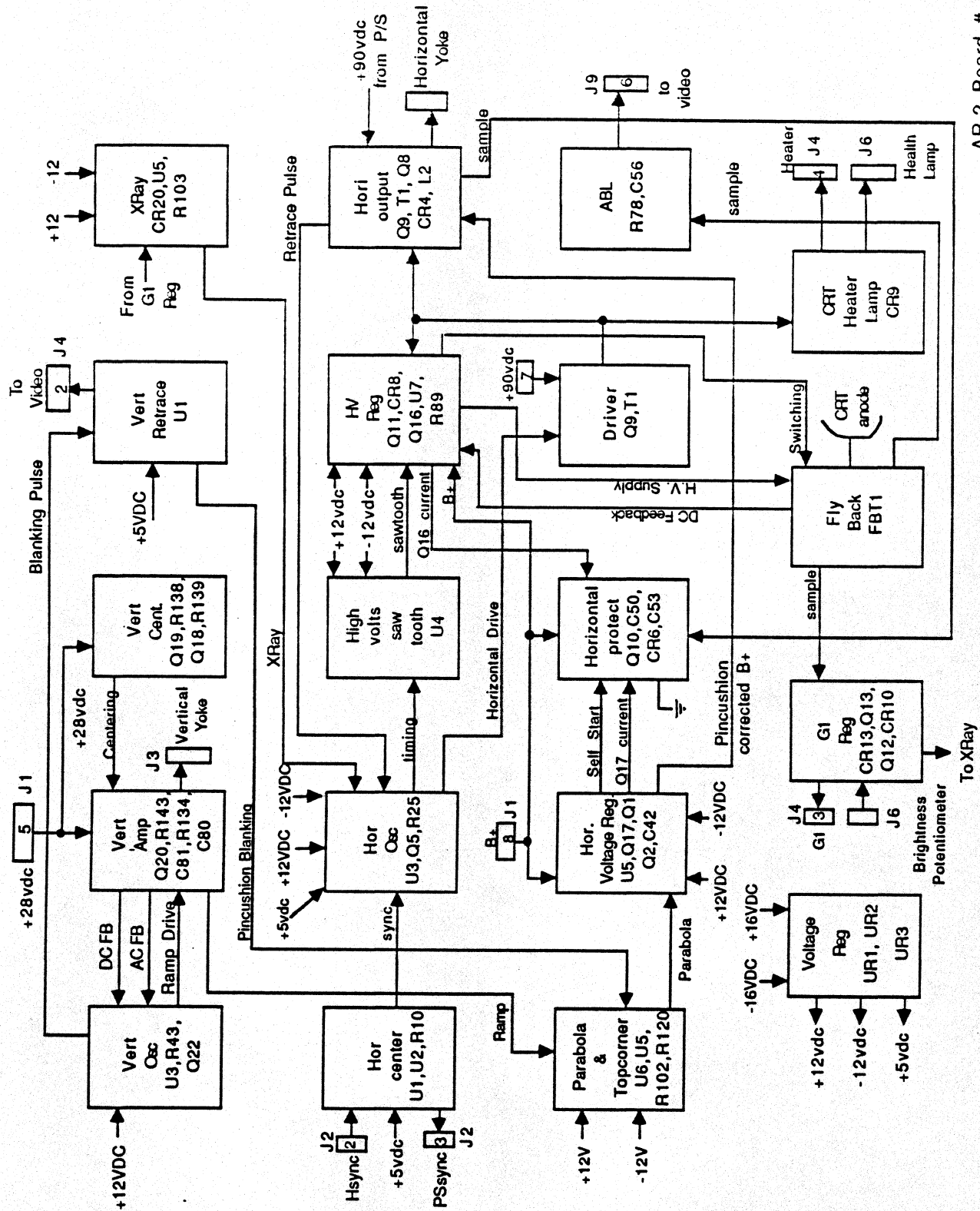


KM-3/4 Deflection Board



KM-3, Board #103302 Schematic #103300
 KM-4 Board #105763 Schematic #105761

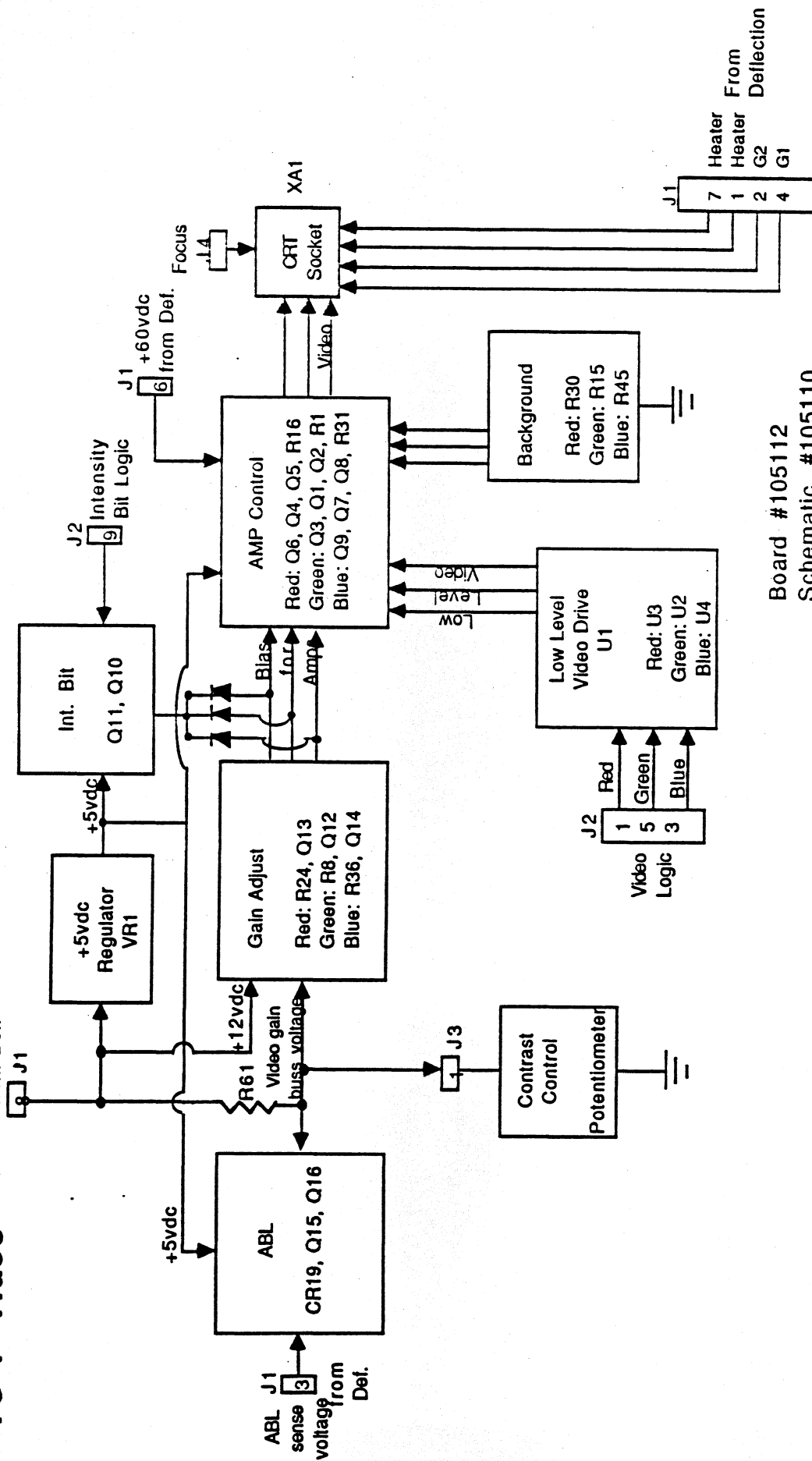
AR-2 Deflection Board



AR-2 Board # 105157
AR-2 Schematic # 105155

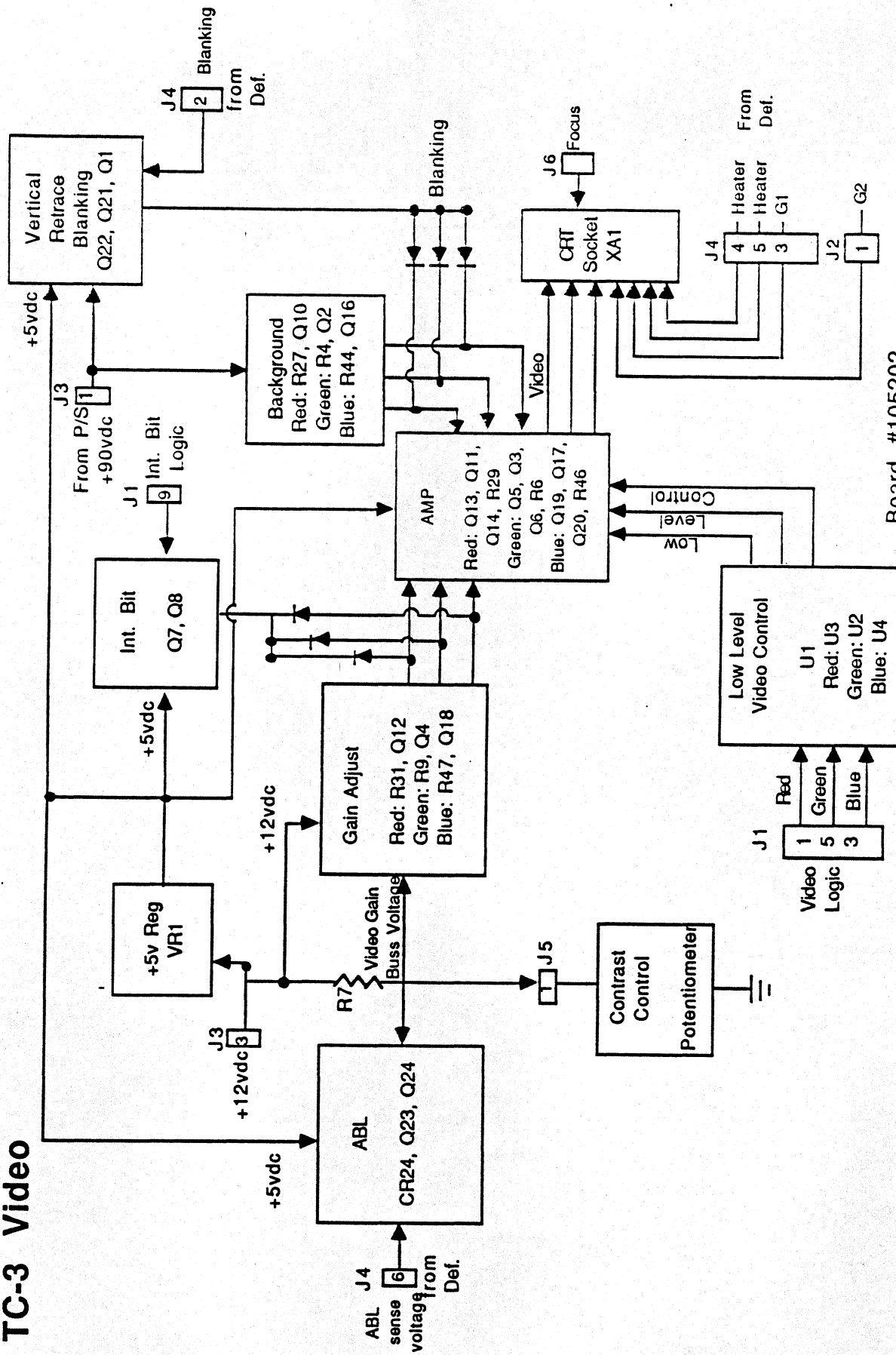
TC-1 Video

+12vdc from Def.



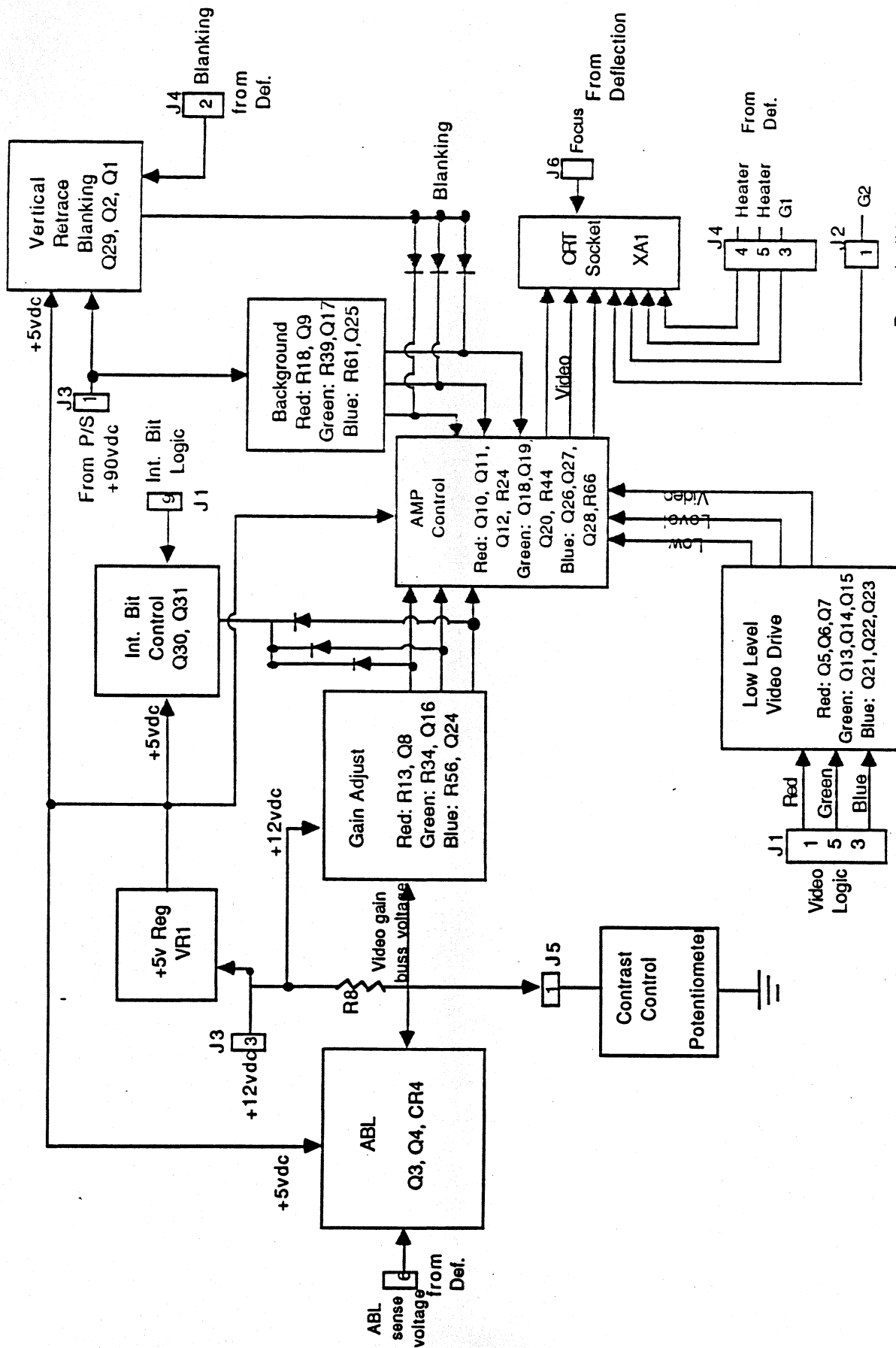
Board #105112
Schematic #105110

TC-3 Video



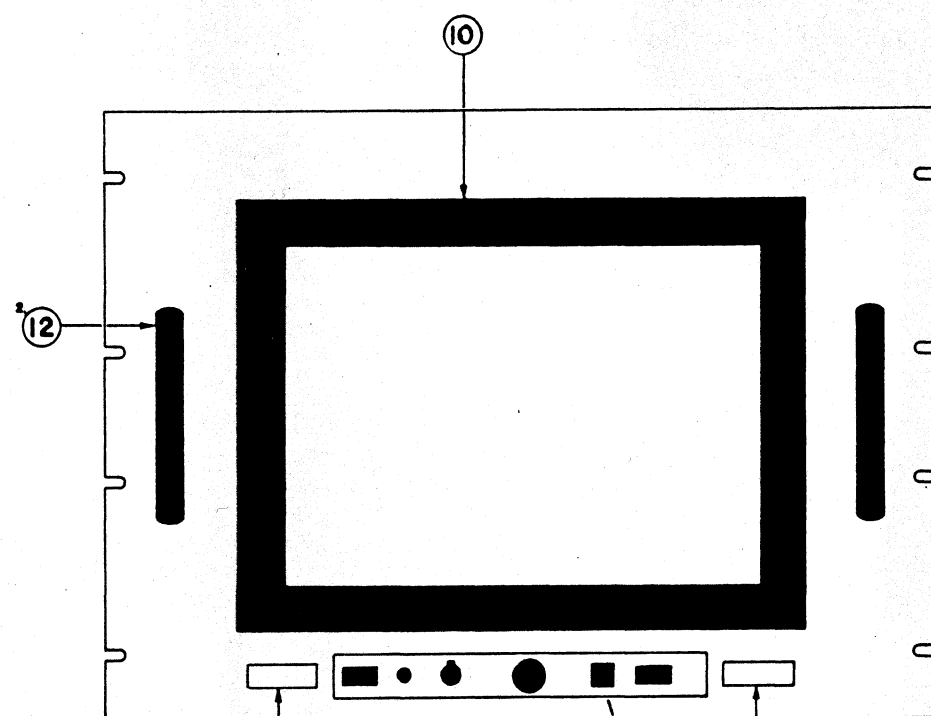
Board #105202
Schematic #105200

AR-2 Video

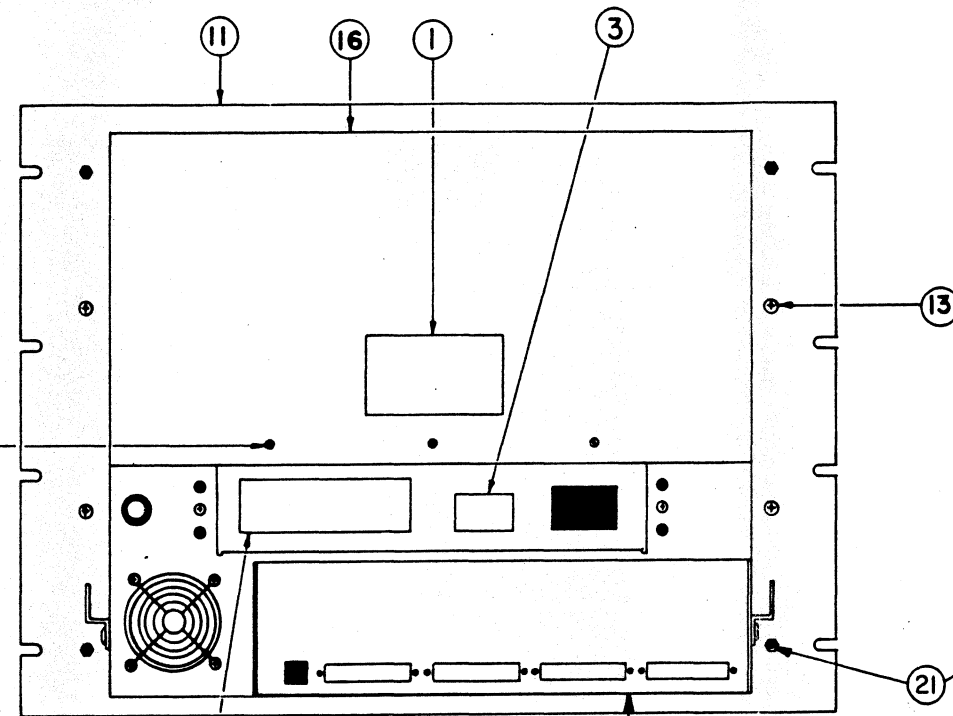


Board #105199
Schematic #105197

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4737	6/5/87	T. JACKSON
2	SEE ECN	4780, 4792	7/27/87	28
3	SEE ECN	4935	6/1/88	6L
4	SEE ECN	5049		



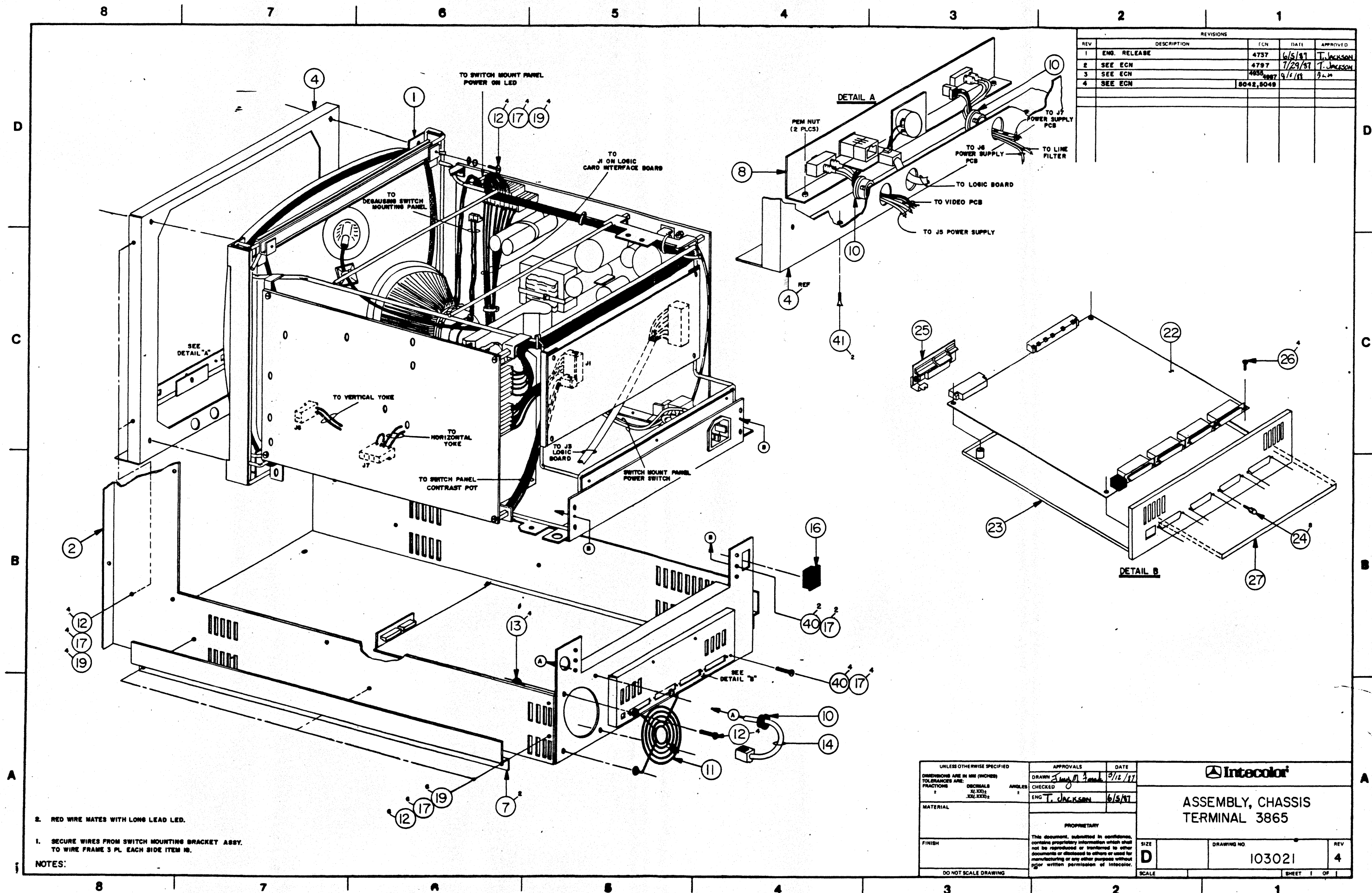
FRONT VIEW



REAR VIEW

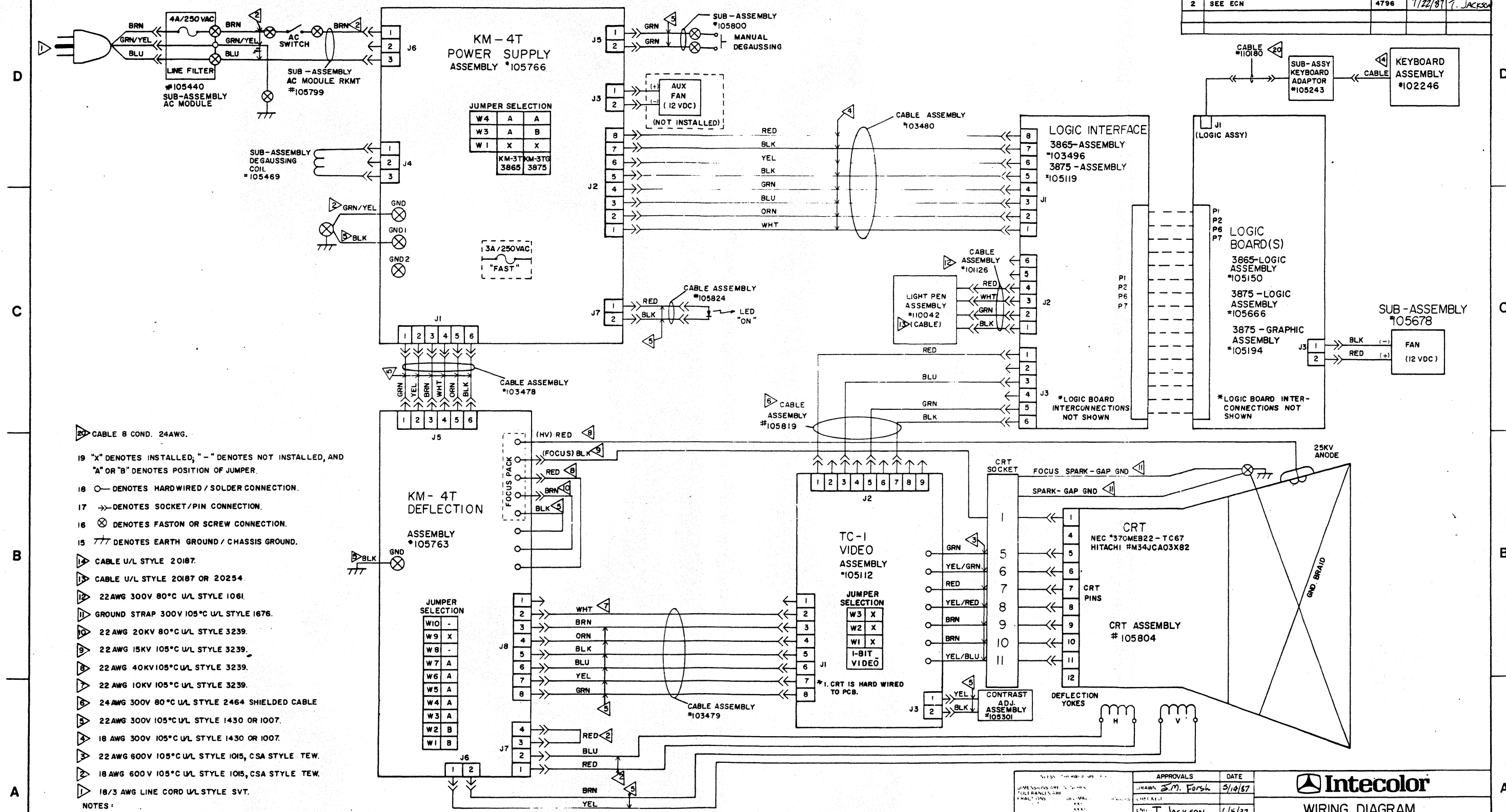
NOTES

UNLESS OTHERWISE SPECIFIED: RESISTORS ARE 1/4 WATT 10% RESISTANCE VALUES ARE IN OHMS CAPACITORS ARE 16V CAPACITANCE VALUES ARE IN MICROFARADS		APPROVALS DRAWN <i>SA</i> 7/2/87 CHECKED ENG. T. JACKSON 6/5/87		DATE	Intecolor TOP ASSEMBLY 3865
PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SIZE D DRAWING NO. 103020 SHEET 4 OF 4		REV 4	



8 7 6 5 4 3 2 1

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4737	6/5/87	T. JACKSON
2	SEE ECN	4796	7/22/87	T. JACKSON



APPROVALS

DATE 5/10/87

DATE 6/5/87

DATE 6/5/87

Intecolor

WIRING DIAGRAM

3865 (ASSY. 103020 REV. 1) /

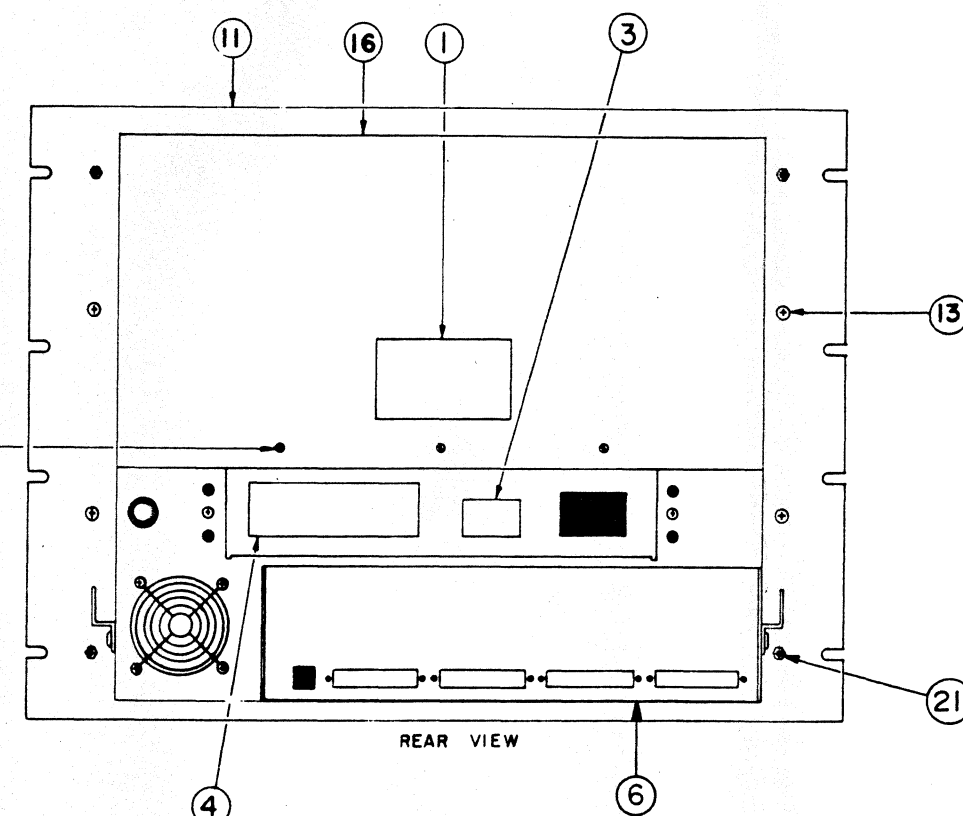
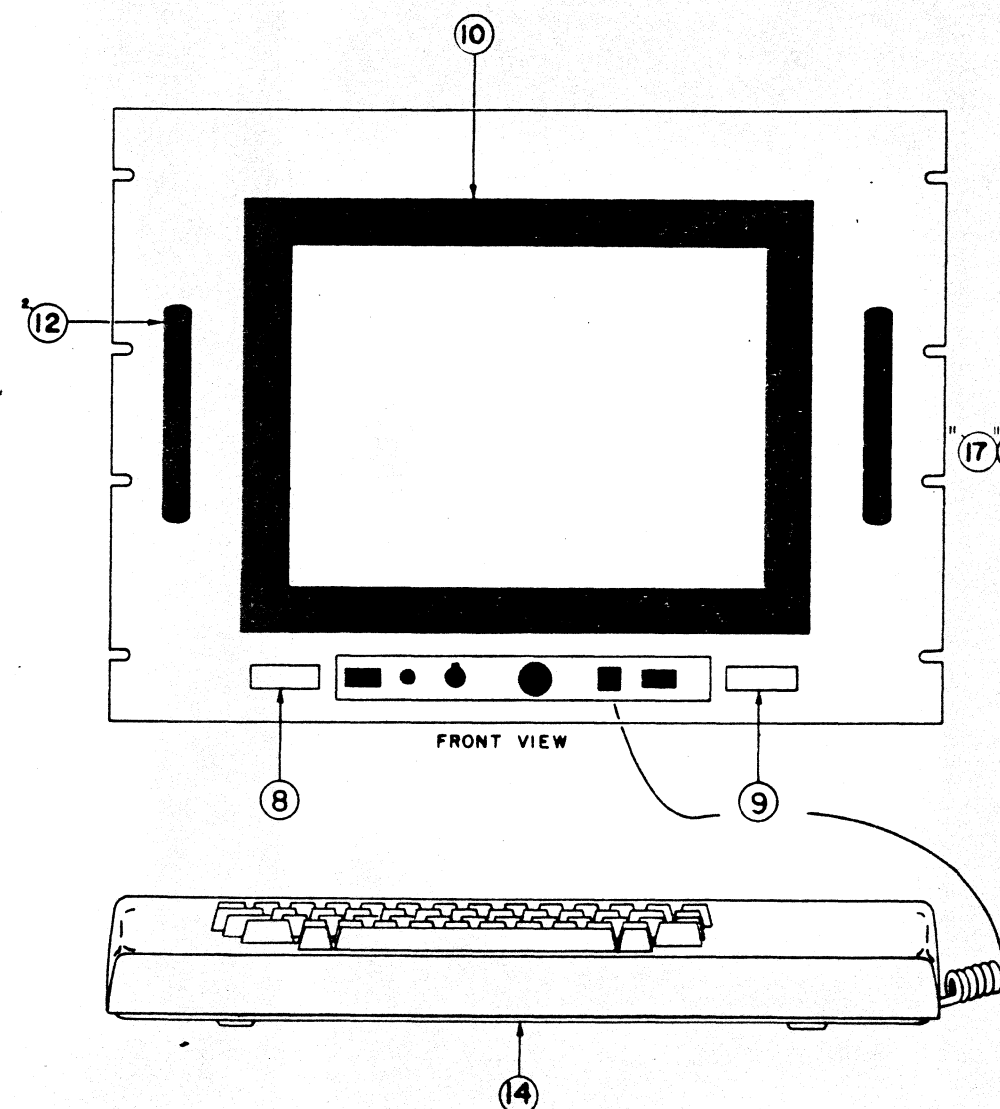
3875 (ASSY. 103024 REV. 1)

SIZE D

DRAWING NO 103022

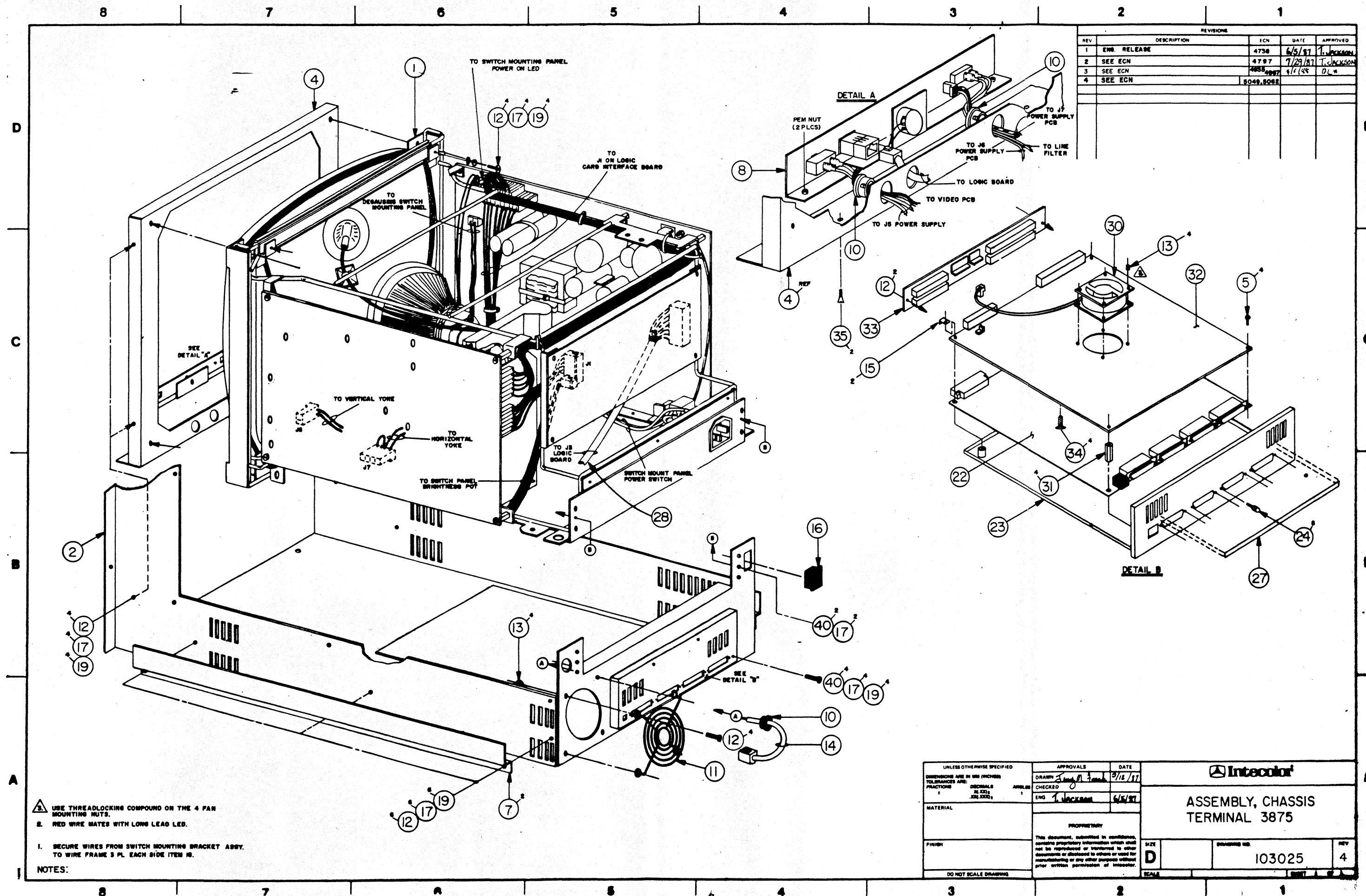
REV 2

REVISIONS				
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3	SEE ECN	4935	9/6/88	ECN
4	SEE ECN	5049		

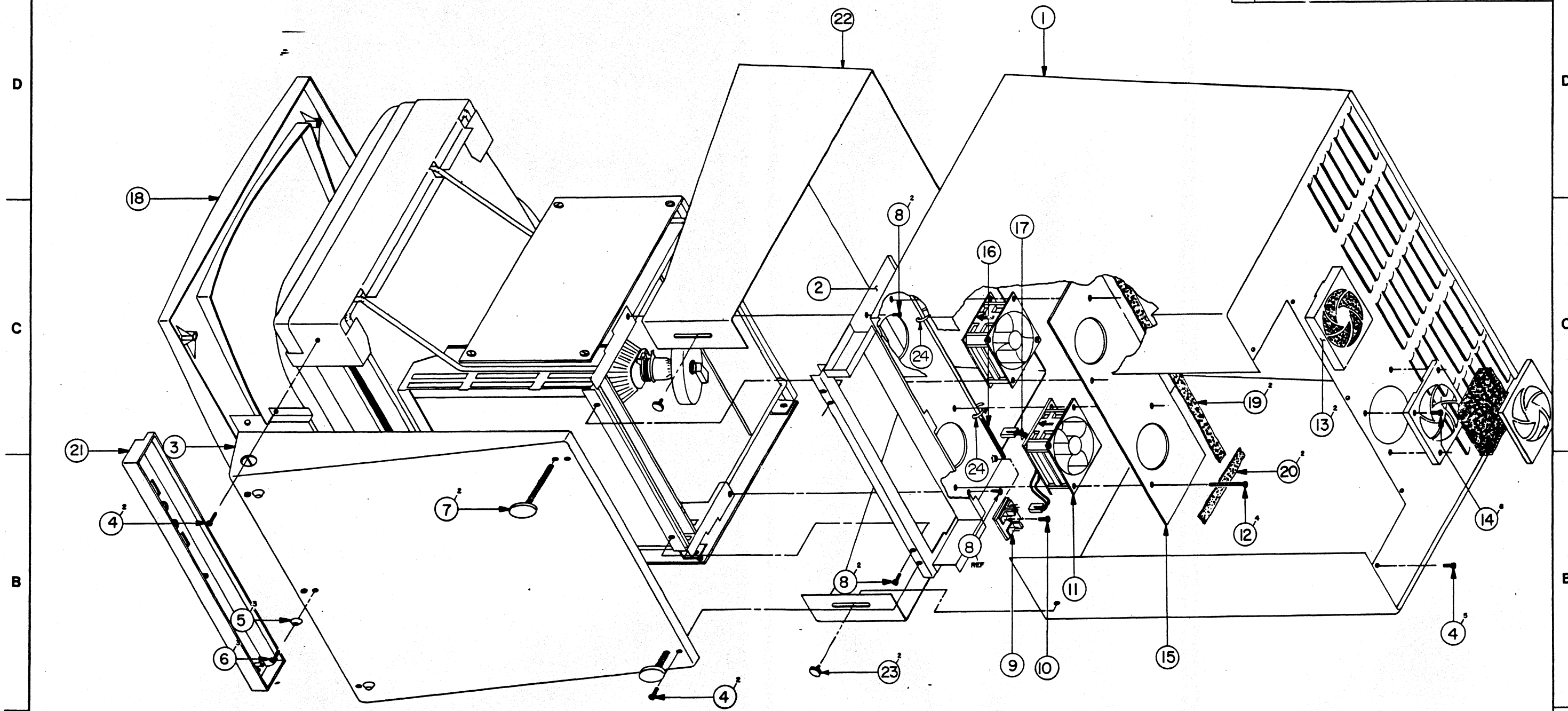


NOTES

UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4 WATT 10% RESISTANCE VALUES ARE IN OHMS CAPACITORS ARE 16V CAPACITANCE VALUES ARE IN MICROFARADS		APPROVALS DRAWN <i>[Signature]</i> 7/4/87 CHECKED ENG. <i>[Signature]</i> 6/5/87		DATE	Intecolor TOP ASSEMBLY 3875
PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SIZE D		DRAWING NO. 103024	
LAST USED NOT USED		DO NOT SCALE DRAWING		SHEET 4	OF 4

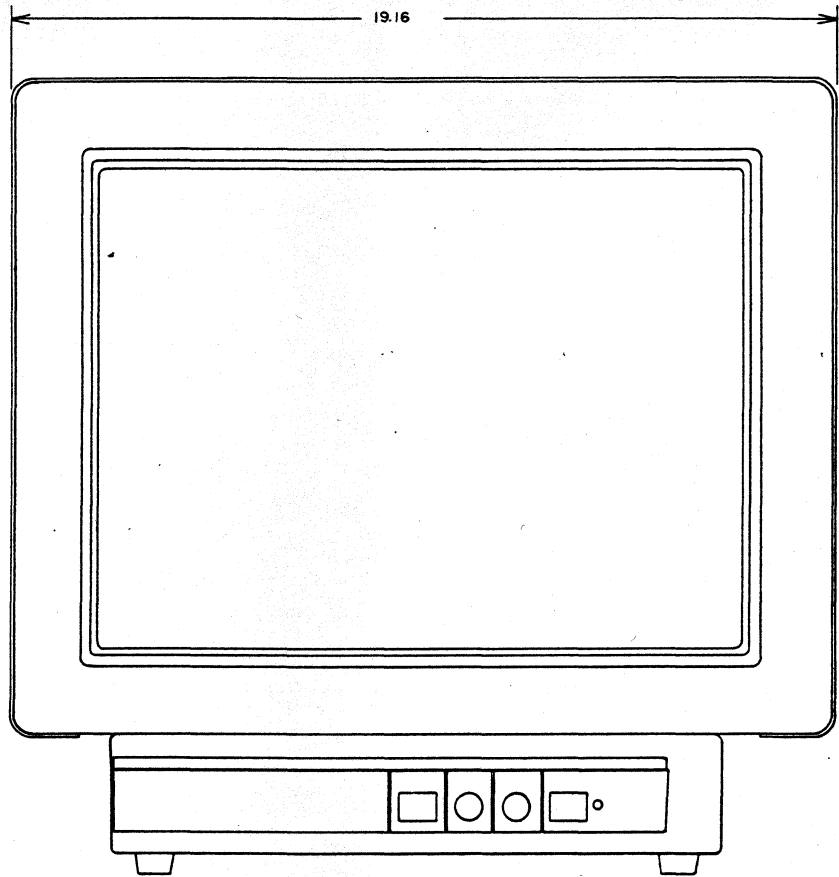


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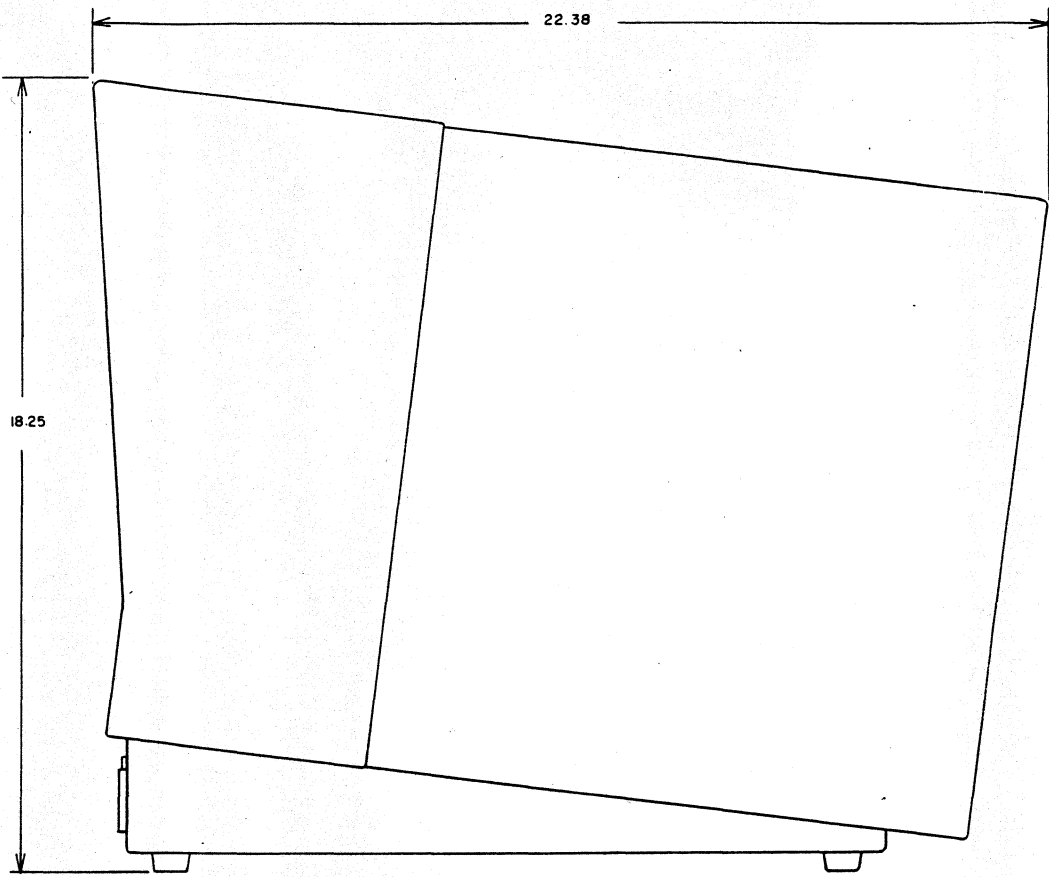


UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN INCHES		DRAWN <i>S. M. Smith</i>		12/1/82	
TOLERANCES ARE:		CHECKED			
FRACTIONS		ENG <i>John H. Smith</i>		2/9/88	
DECIMALS					
ANGLES					
MATERIAL					
FINISH					
DO NOT SCALE DRAWING					
ASSEMBLY NEMA 2 ENCLOSURE					
SIZE	D	DRAWING NO.	103119		REV
SCALE		SHEET		1	OF

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4902	2/9/84	OK



FRONT VIEW



SIDE VIEW

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN INCHES		DRAWN BWS		12-2-87	
TOLERANCES ARE:		CHECKED			
FRACTIONS	DECIMALS	ANGLES	ENG. APPROVAL	2/9/84	ENVELOPE DRAWING NEMA 2 ENCLOSURE
- 2	.XX(X)2	2			
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			SIZE D
FINISH		DO NOT SCALE DRAWING			DRAWING NO. 103120
					REV 1
					SCALE SHEET 1 OF 2

8

7

6

5

4

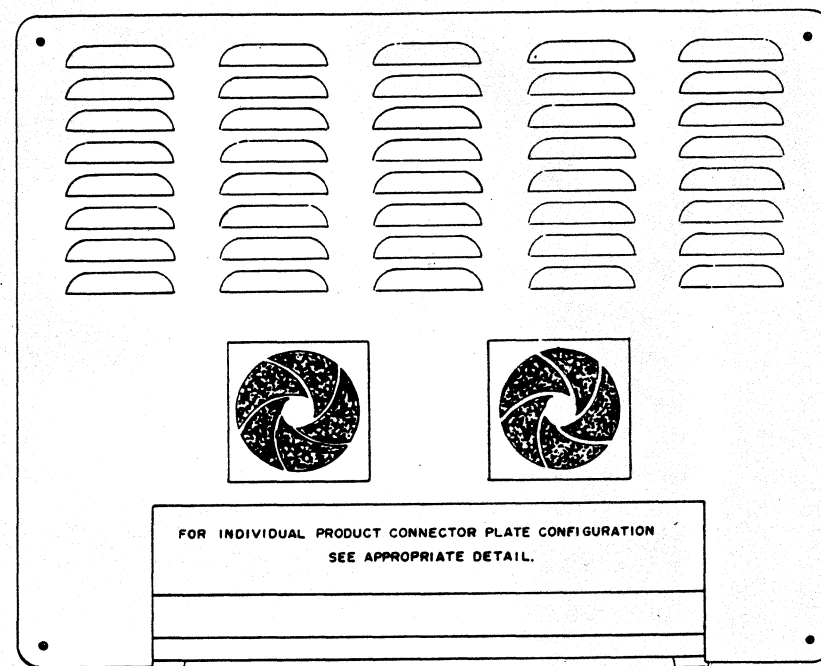
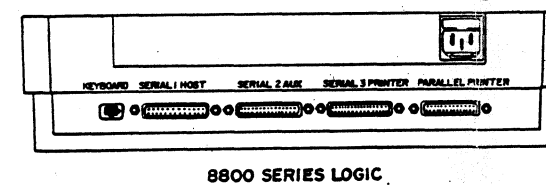
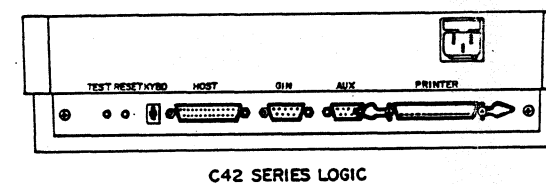
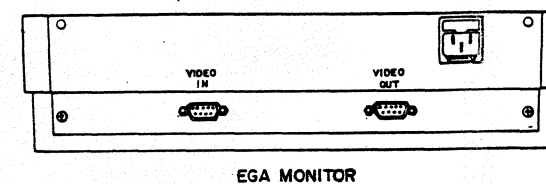
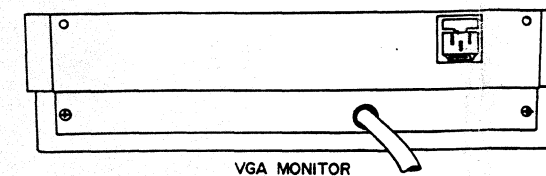
3

2

1

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4902	2/8/84	RLH

CONNECTOR PLATE CONFIGURATIONS



REAR VIEW

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN MM (INCHES)		DRAWN SWB		12-2-87	
TOLERANCES ARE:		CHECKED			
FRACTIONS		ENG [Signature]		2/8/84	
MATERIAL		PROPRIETARY			
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			
DO NOT SCALE DRAWING		SIZE D		DRAWING NO. 103120	
		SCALE		REV 1	
				SHEET 2 OF 2	

8

7

6

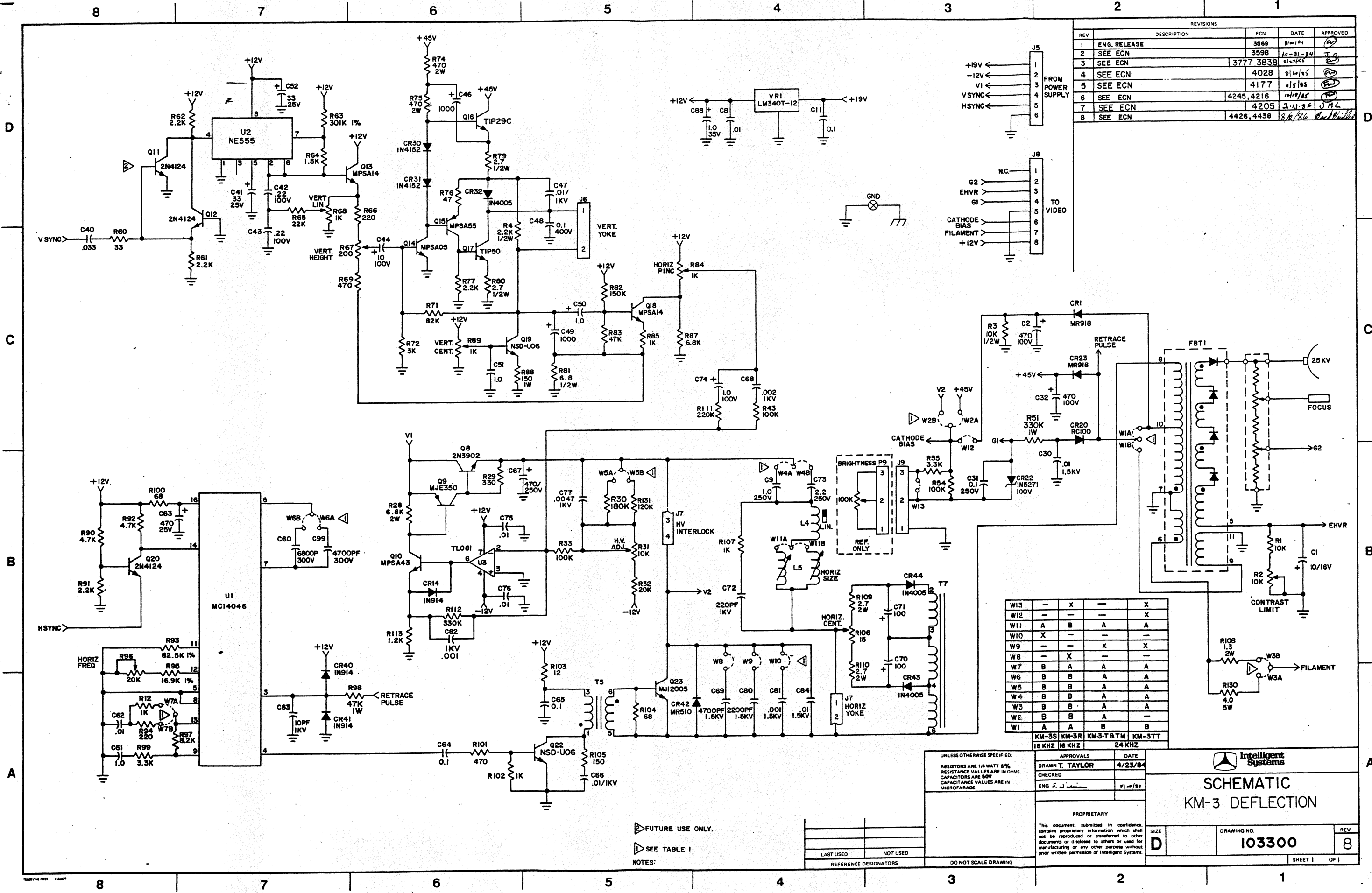
5

4

3

2

1



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	3569	8/1/84	
2	SEE ECN	3598	10-31-84	
3	SEE ECN	3777 3838	11-17-85	
4	SEE ECN	4028	8/24/85	
5	SEE ECN	4177	11/5/85	
6	SEE ECN	4245, 4216	10/19/85	
7	SEE ECN	4205	2-11-86	
8	SEE ECN	4426, 4438	8/4/86	

W13	-	X	-	X
W12	-	-	-	X
W11	A	B	A	A
W10	X	-	-	-
W9	-	-	X	X
W8	-	X	-	-
W7	B	A	A	A
W6	B	B	A	A
W5	B	B	A	A
W4	B	B	A	A
W3	B	B	A	A
W2	B	B	A	-
W1	A	A	B	B

KM-3S	KM-3R	KM-3T8TM	KM-3TT
18 KHZ	16 KHZ	24 KHZ	

APPROVALS		DATE
DRAWN T. TAYLOR	CHECKED	4/23/84
ENG. F. J. JONES		8/1/84

PROPRIETARY
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SCHEMATIC
KM-3 DEFLECTION

SIZE
D

DRAWING NO.
103300

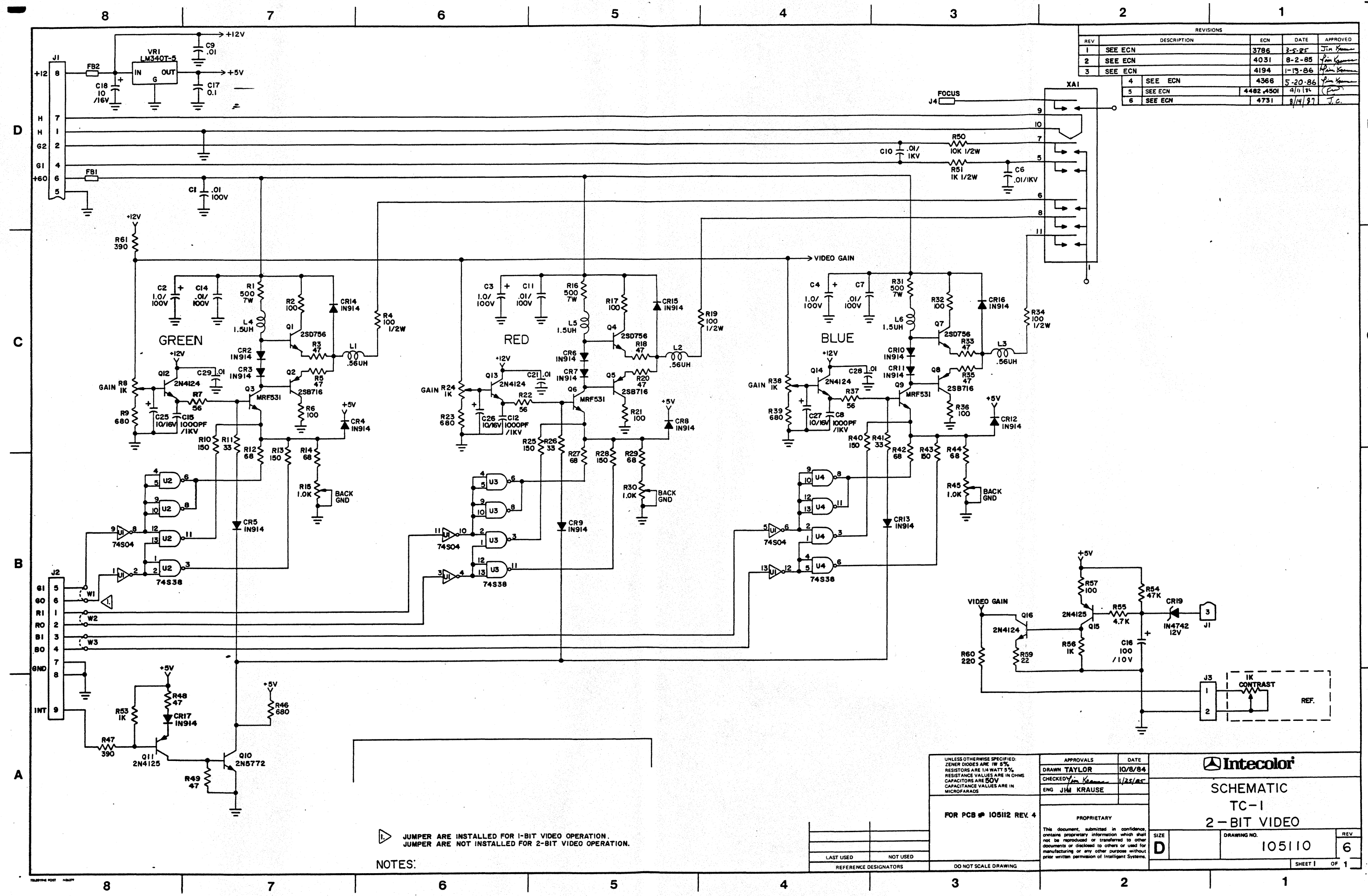
REV
8

SHEET 1

OF 1

NOTES:
▶ FUTURE USE ONLY.
▶ SEE TABLE I

REFERENCE DESIGNATORS		DO NOT SCALE DRAWING	
LAST USED	NOT USED		



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	SEE ECN	3786	3-5-85	Jim Krause
2	SEE ECN	4031	8-2-85	Jim Krause
3	SEE ECN	4194	1-13-86	Jim Krause
4	SEE ECN	4366	5-20-86	Jim Krause
5	SEE ECN	4482, 4501	4/11/87	Jim Krause
6	SEE ECN	4731	8/14/87	J.C.

NOTES:
JUMPER ARE INSTALLED FOR 1-BIT VIDEO OPERATION.
JUMPER ARE NOT INSTALLED FOR 2-BIT VIDEO OPERATION.

UNLESS OTHERWISE SPECIFIED:
ZENER DIODES ARE 1W 5%
RESISTORS ARE 1/4 WATT 5%
RESISTANCE VALUES ARE IN OHMS
CAPACITORS ARE 50V
CAPACITANCE VALUES ARE IN MICROFARADS

FOR PCB # 105112 REV. 4

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN TAYLOR	10/8/84
CHECKED <i>Jim Krause</i>	1/25/85
ENG JIM KRAUSE	

PROPRIETARY

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Intecolor

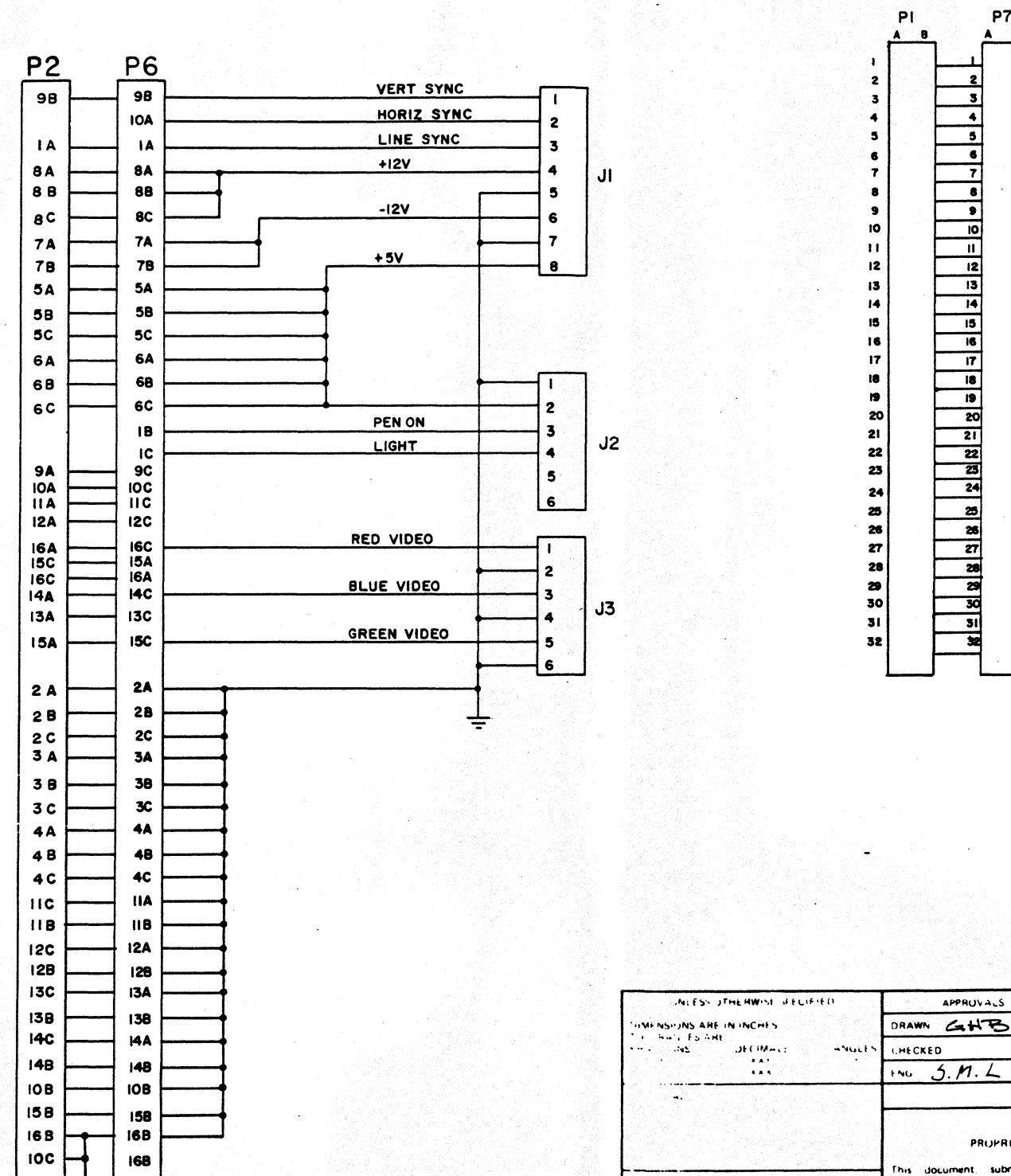
SCHMATIC
TC-1
2-BIT VIDEO

SIZE	D	DRAWING NO.	105110	REV	6
------	---	-------------	--------	-----	---

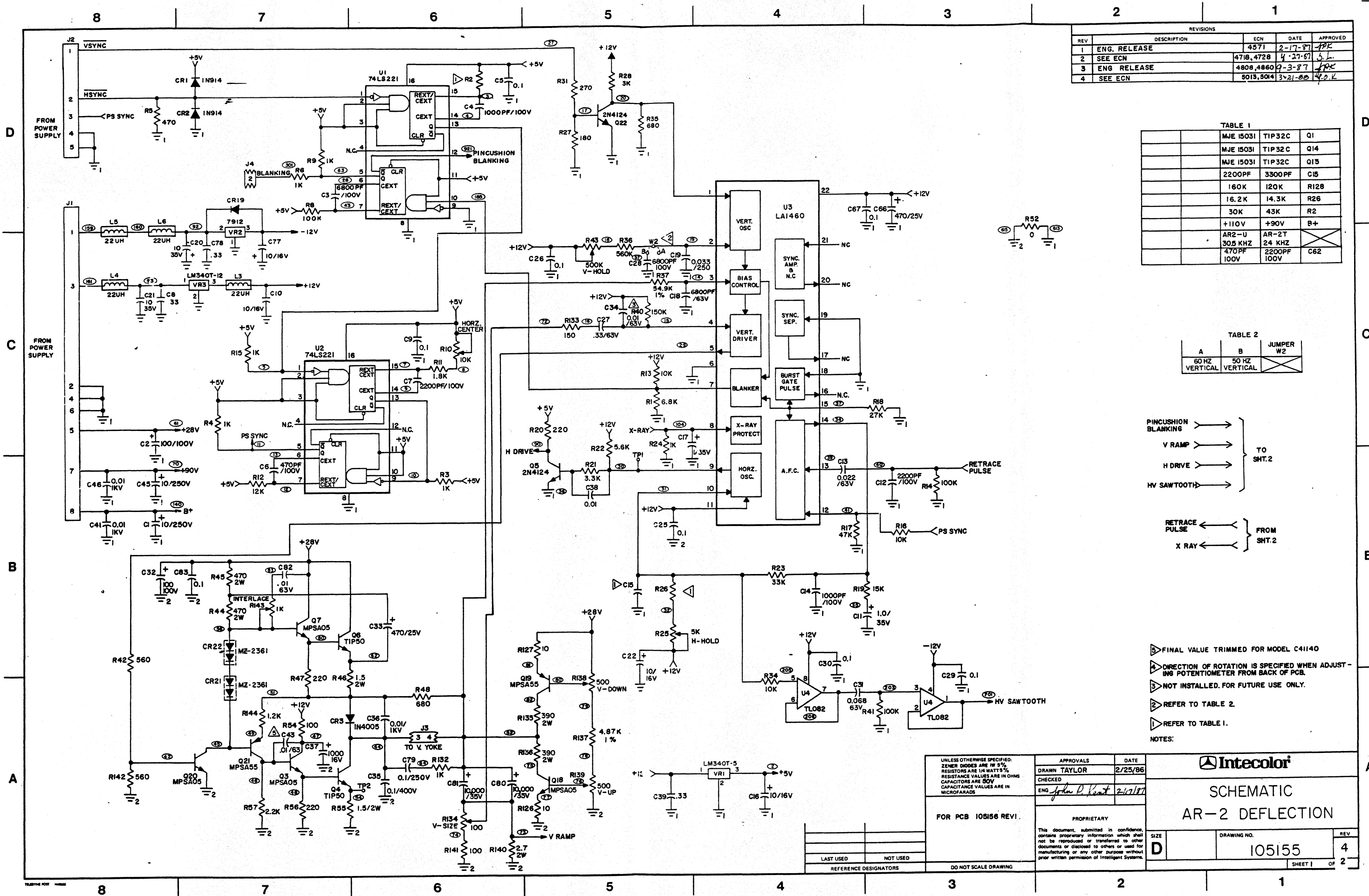
SHEET 1 OF 1

TELETYPE PORT HS27P

REVISIONS				
REV	DESCRIPTION	ECN	APPROVED	DATE
1	ENG. RELEASE	3632	J.M.L.	2/3/86



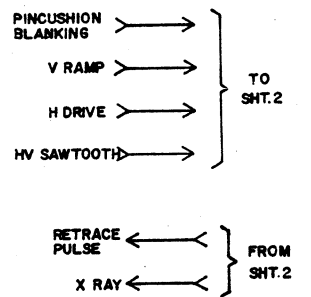
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES 1/16 1/32 1/64 .001 .005 .010 .015 .020 .030 .040 .050 .060 .070 .080 .090 .100 .125 .150 .175 .200 .250 .300 .375 .500 .625 .750 .875 1.000 1.250 1.500 1.750 2.000 2.500 3.000 3.500 4.000 4.500 5.000 5.500 6.000 6.500 7.000 7.500 8.000 8.500 9.000 9.500 10.000		APPROVALS DRAWN <i>GHB</i> CHECKED ENG. <i>J.M.L.</i>	DATE 10-9-84 2-13-86		
SCHEMATIC LOGIC MOTHER BOARD 3820 SERIES				DRAWING NO 105117	
DO NOT SCALE DRAWING		PROPRIETARY This document submitted in confidence contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems.		SIZE C	REV 1
SCALE NTS		SHEET 1 OF 1			



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4571	2-17-87	JPK
2	SEE ECN	4718, 4728	4-27-87	J.L.
3	ENG. RELEASE	4808, 4860	9-3-87	JPK
4	SEE ECN	5015, 5044	3-21-88	J.L.

TABLE 1			
	MJE 15031	TIP32C	Q1
	MJE 15031	TIP32C	Q14
	MJE 15031	TIP32C	Q15
	2200PF	3300PF	C15
	160K	120K	R128
	16.2K	14.3K	R2
	30K	43K	R26
	+110V	+90V	B+
	AR2-U	AR-2T	
	30.5 KHZ	24 KHZ	
	470PF	2200PF	C62
	100V	100V	

TABLE 2		
A	B	JUMPER W2
60 HZ	50 HZ	
VERTICAL	VERTICAL	



- 5 FINAL VALUE TRIMMED FOR MODEL C41140
 - 4 DIRECTION OF ROTATION IS SPECIFIED WHEN ADJUSTING POTENTIOMETER FROM BACK OF PCB.
 - 3 NOT INSTALLED, FOR FUTURE USE ONLY.
 - 2 REFER TO TABLE 2.
 - 1 REFER TO TABLE 1.
- NOTES:

UNLESS OTHERWISE SPECIFIED:
ZENER DIODES ARE 1W 5%
RESISTORS ARE 1/4 WATT 5%
RESISTANCE VALUES ARE IN OHMS
CAPACITORS ARE 50V
CAPACITANCE VALUES ARE IN MICROFARADS

FOR PCB 105156 REV1.

APPROVALS

DRAWN TAYLOR

CHECKED

ENG John P. Keast

PROPRIETARY

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DATE

2/25/86

2/27/87

Intecolor

SCHEMATIC

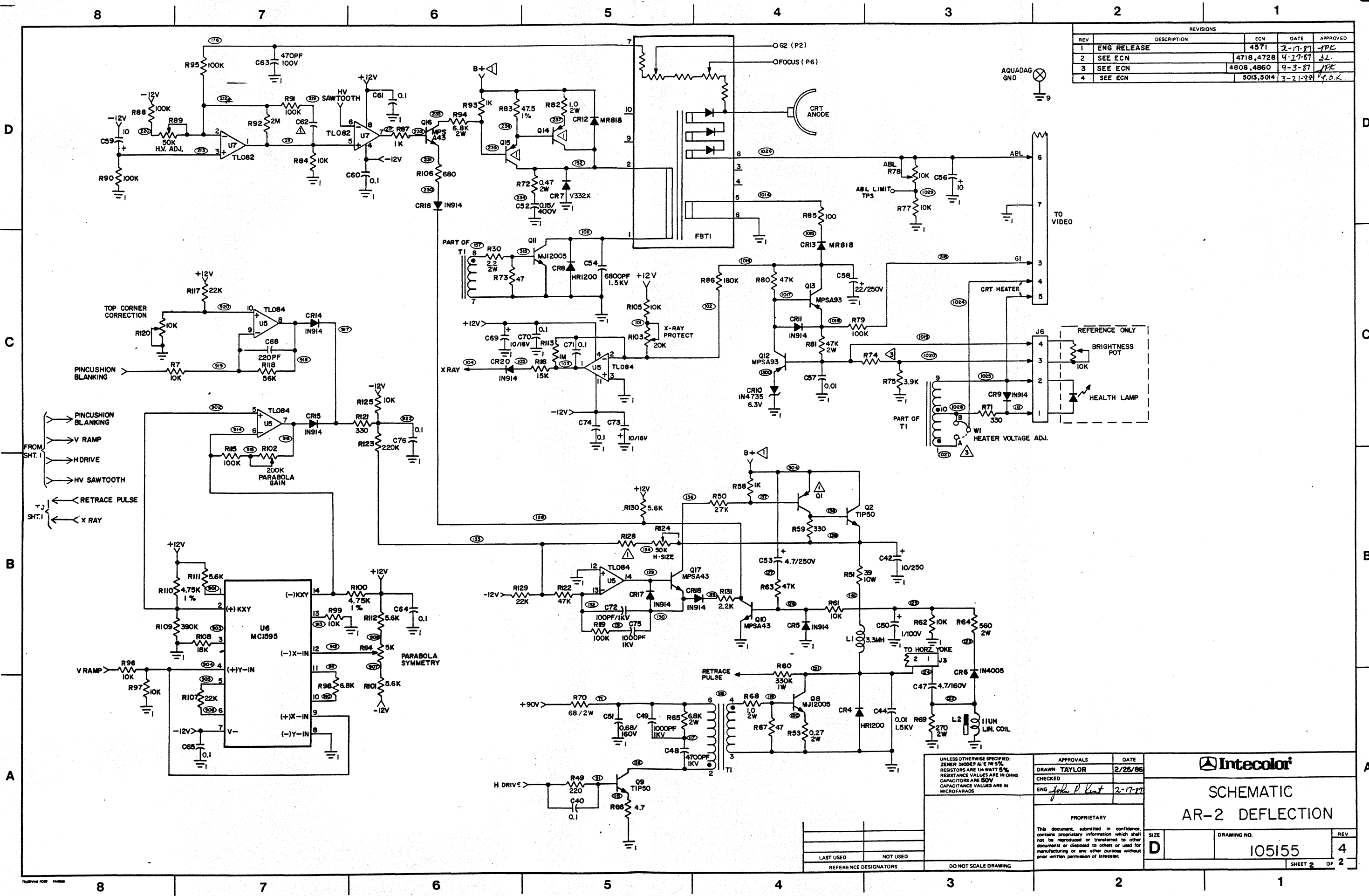
AR-2 DEFLECTION

SIZE D

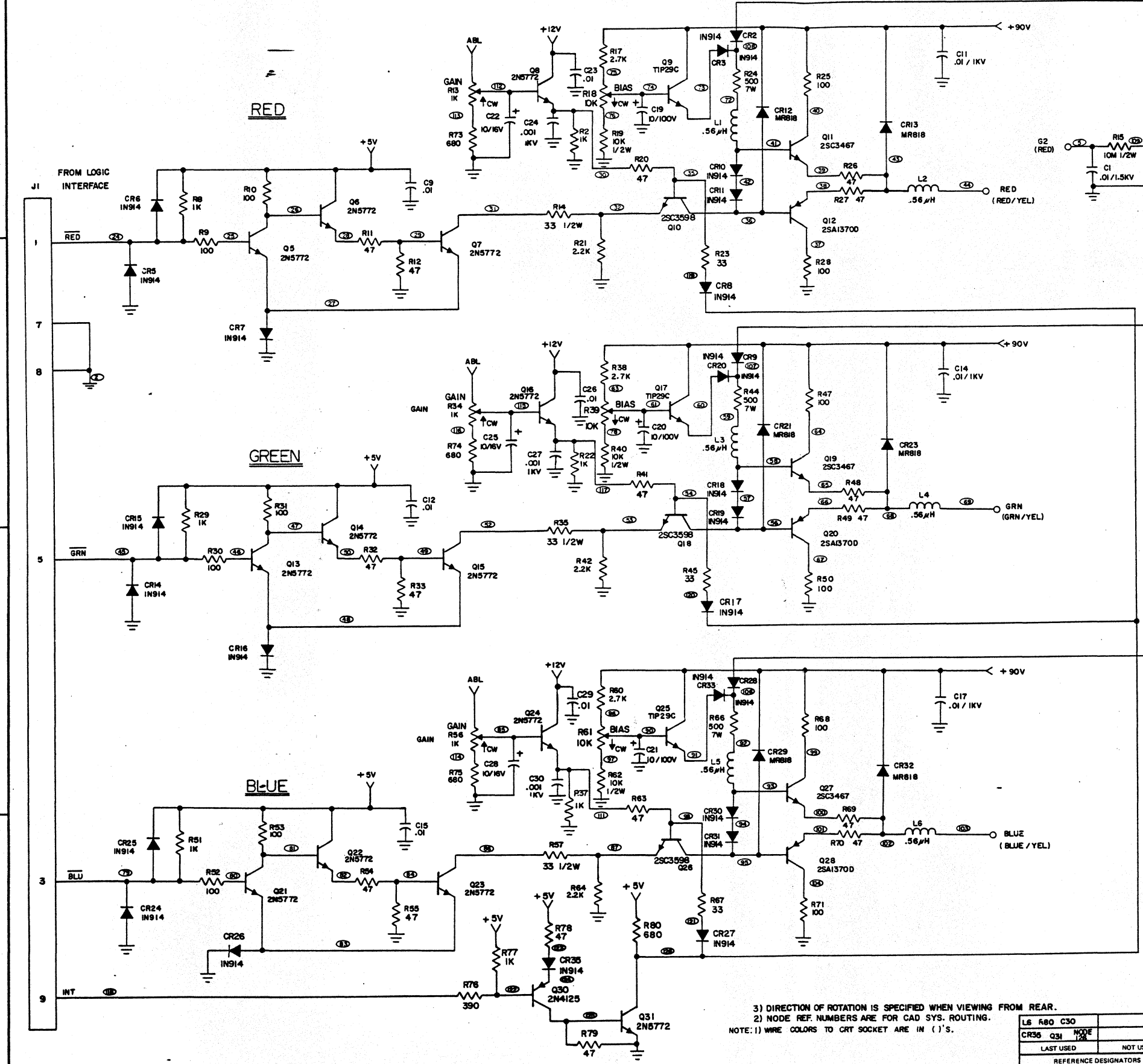
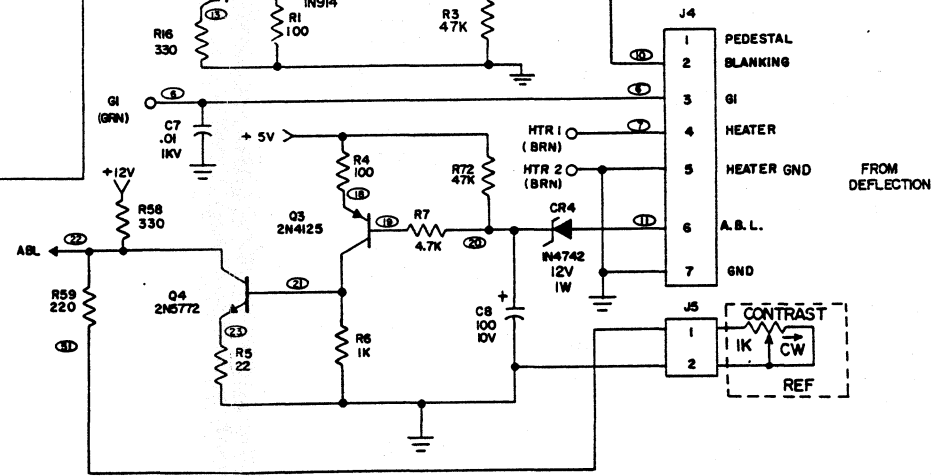
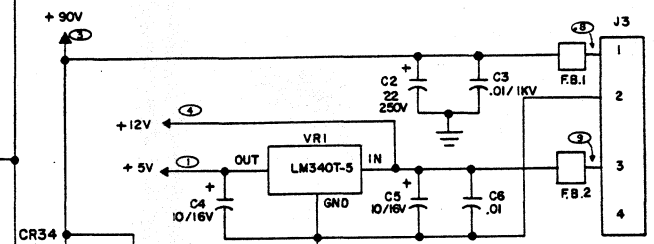
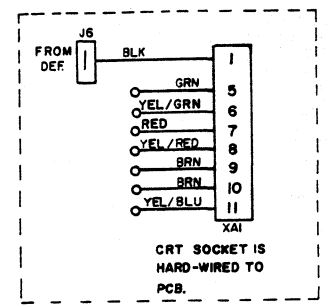
DRAWING NO. 105155

REV 4

SHEET 1 OF 2



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	3840	2-10-87	J.D.K.



3) DIRECTION OF ROTATION IS SPECIFIED WHEN VIEWING FROM REAR.
2) NODE REF. NUMBERS ARE FOR CAD SYS. ROUTING.
NOTE: 1) WIRE COLORS TO CRT SOCKET ARE IN ()'S.

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 1/4 WATT 5%
RESISTANCE VALUES ARE IN OHMS
CAPACITORS ARE .001
CAPACITANCE VALUES ARE IN MICROFARADS

APPROVALS
DRAWN BY MOORE
CHECKED
ENG J. K. K.

DATE
1-6-86
2-10-87

PROPRIETARY

FOR PCB 105198 REV 1

DO NOT SCALE DRAWING

Intecolor

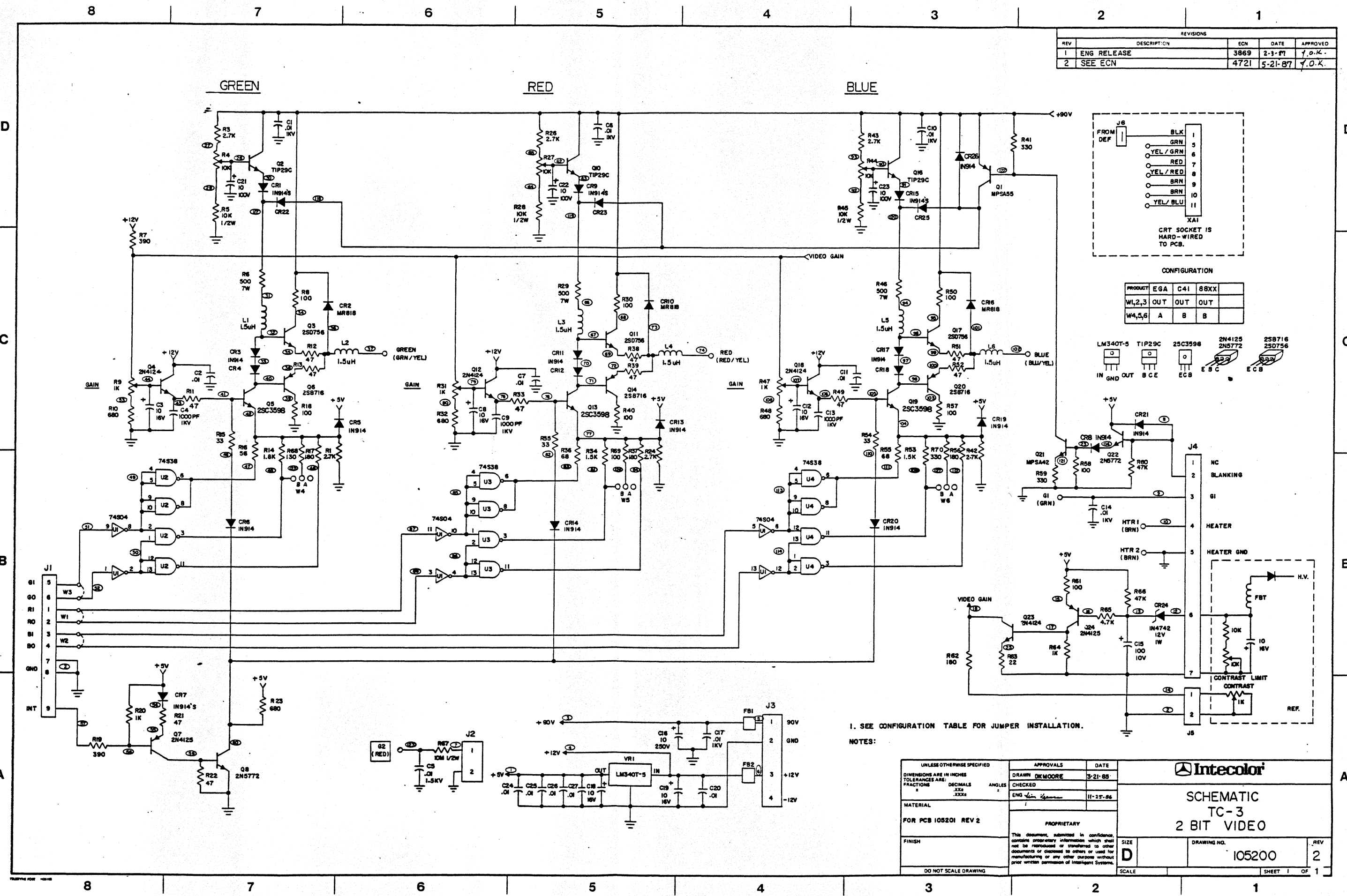
SCHEMATIC
AR-2 VIDEO

SIZE
D

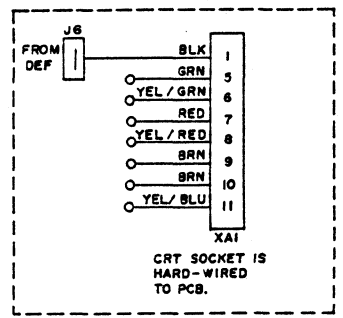
DRAWING NO.
105197

REV
1

SHEET 1 OF 1

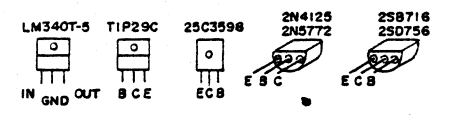


REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	3869	2-3-87	J.P.K.
2	SEE ECN	4721	5-21-87	J.P.K.



CONFIGURATION

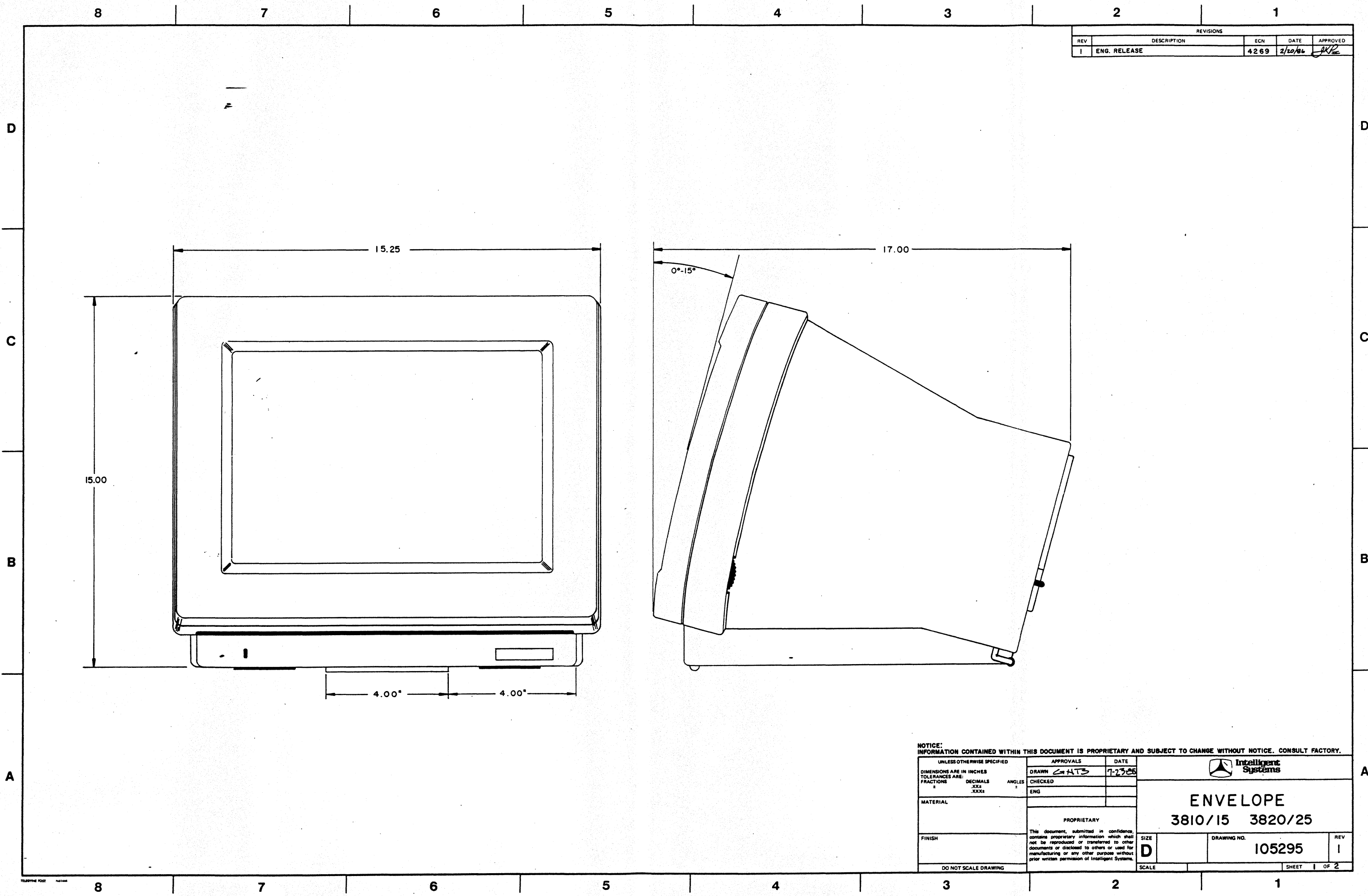
PRODUCT	EGA	C41	88XX
WL2,3	OUT	OUT	OUT
W4,5,6	A	B	B



1. SEE CONFIGURATION TABLE FOR JUMPER INSTALLATION.

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XXx 2	APPROVALS	DATE
	DRAWN OK MOORE	3-21-88
	CHECKED	
	ENG J. P. K.	11-25-88
MATERIAL	PROPRIETARY	
FOR PCB 105201 REV 2	This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Inteligent Systems.	
FINISH	SIZE D	DRAWING NO. 105200
DO NOT SCALE DRAWING	SCALE	SHEET 1 OF 1



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4269	2/10/86	JK/SC

NOTICE: INFORMATION CONTAINED WITHIN THIS DOCUMENT IS PROPRIETARY AND SUBJECT TO CHANGE WITHOUT NOTICE. CONSULT FACTORY.		
UNLESS OTHERWISE SPECIFIED	APPROVALS	DATE
DIMENSIONS ARE IN INCHES	DRAWN <i>CHS</i>	7-23-85
TOLERANCES ARE:	CHECKED	
FRACTIONS	ENG	
DECIMALS		
ANGLES		
MATERIAL		
FINISH		
DO NOT SCALE DRAWING		
PROPRIETARY		
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INTELLIGENT SYSTEMS		
ENVELOPE		
3810/15 3820/25		
SIZE	DRAWING NO.	REV
D	105295	1
SCALE	SHEET 1 OF 2	

8

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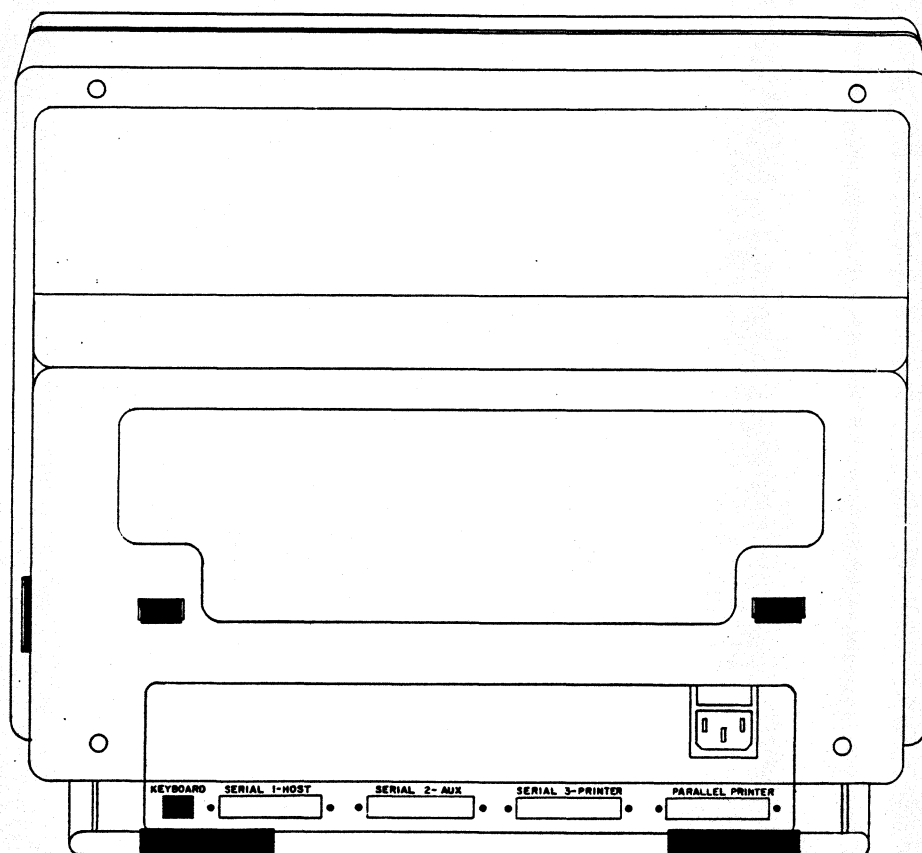
4

3

2

1

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4269	2/10/66	JLR



NOTICE: INFORMATION CONTAINED WITHIN THIS DOCUMENT IS PROPRIETARY AND SUBJECT TO CHANGE WITHOUT NOTICE. CONSULT FACTORY.			
UNLESS OTHERWISE SPECIFIED		APPROVALS	DATE
DIMENSIONS ARE IN INCHES		DRAWN <i>ENT</i>	7-22-65
TOLERANCES ARE:		CHECKED	
FRACTIONS	DECIMALS	ANGLES	ENG
±	.XX±	±	
MATERIAL		PROPRIETARY	
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems.	
DO NOT SCALE DRAWING		SIZE D	DRAWING NO. 105295
		SCALE	SHEET 2 OF 2



ENVELOPE
3810/15 3820/25

105295

REV 1

TO J6 ON PCB
POWER SUPPLY

3

BROWN

BLU

TO POWER SUPPLY

POWER SWITCH

REF

13

REF

1

24

GRN/YEL

14

DETAIL A

NOTES:

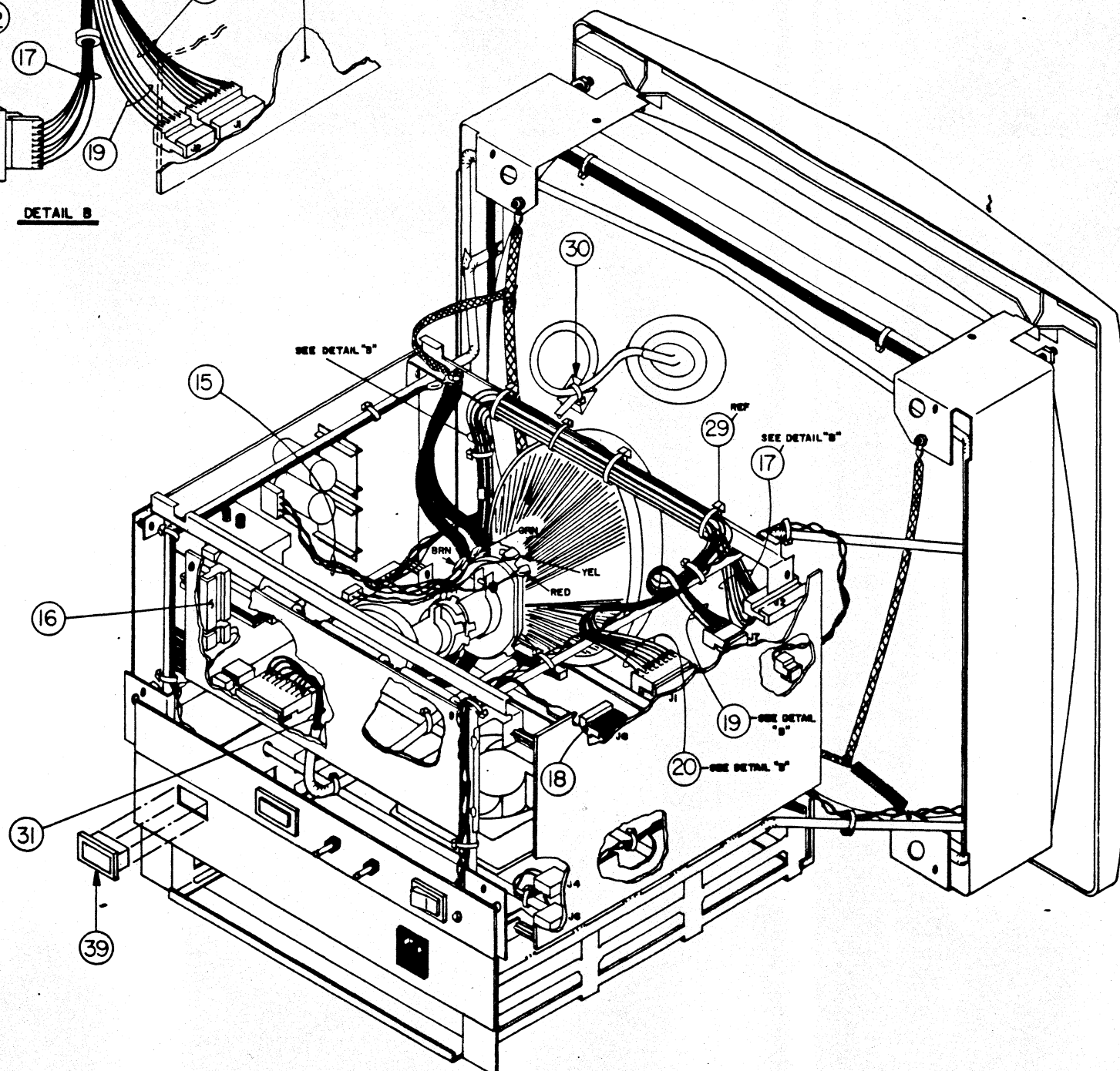
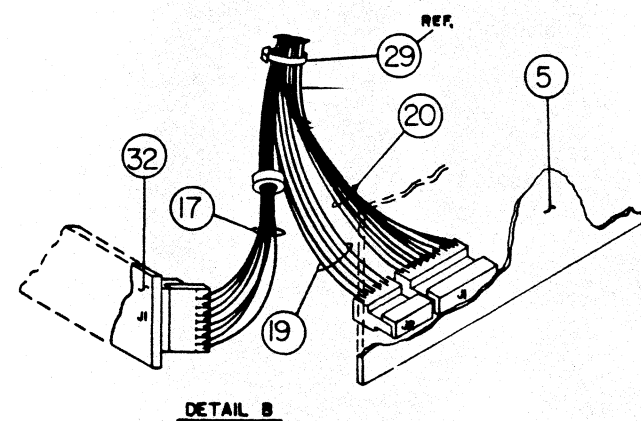
⚠ COVER EDGE OF METAL WITH CATERPILLAR GROMMET ITEM 27.

⚠ UNIT MUST BE BURNED IN, TESTED, AND SHIPPED WITH THE SAME LINE CODE.

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE					
DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES XX: XXXY		DRAWN <i>E.M. Lorch</i>		7/5/66					
		CHECKED							
MATERIAL		ENG <i>James Hight</i>		<i>Wilder</i>		CHASSIS ASSEMBLY CMR - 2			
FINISH		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SIZE				DRAWING NO.	
				D				105429	
DO NOT SCALE DRAWING				SCALE		SHEET 1 OF 1			

8 7 6 5 4 3 2 1

REVISIONS				
REV	DESCRIPTION	ICN	DATE	APPROVED
1	ENG. RELEASE	4379	11/3/86	DLH
2	SEE ECN	4702	9/11/87	DLH
3	SEE ECN	4773	6/12/87	DLH
4	SEE ECN	4823, 4835	9-21-87	YOK
5	SEE ECN	4914, 4915	11/20/88	J.C.
6	SEE ECN	4998	5-10-88	YOK
7	SEE ECN	6025, 6031	5-24-88	J.C.

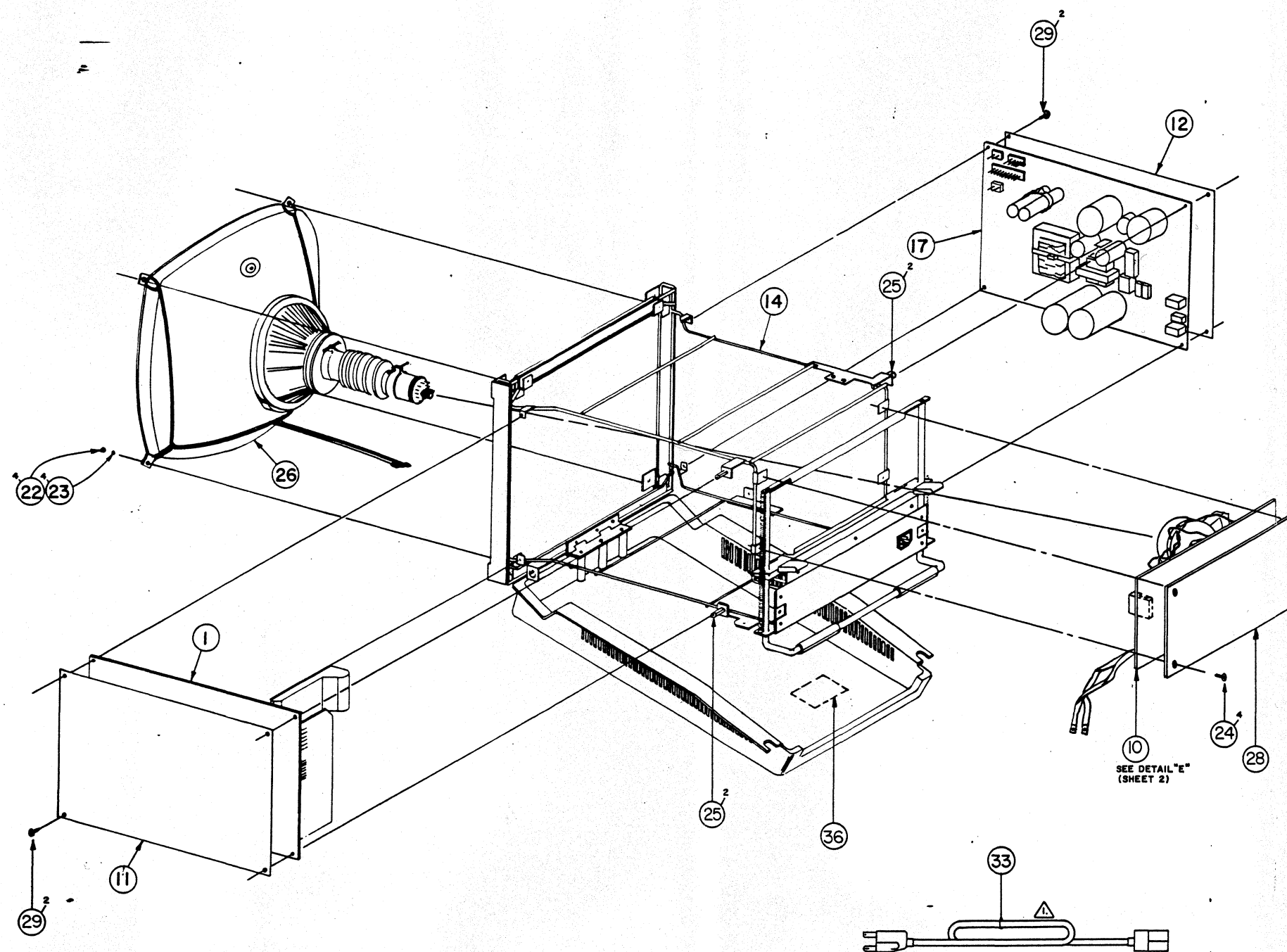


UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN INCHES		DRAWN <i>[Signature]</i>		11/20/86	
TOLERANCES ARE:		CHECKED			
FRACTIONS		ENG <i>[Signature]</i>		11/21/87	
DECIMALS					
ANGLES					
MATERIAL					
FINISH					
DO NOT SCALE DRAWING					

Intecolor	
CHASSIS ASSEMBLY CMR- 2	
SIZE D	DRAWING NO. 105429
REV 7	SHEET 2 OF 2

8 7 6 5 4 3 2 1

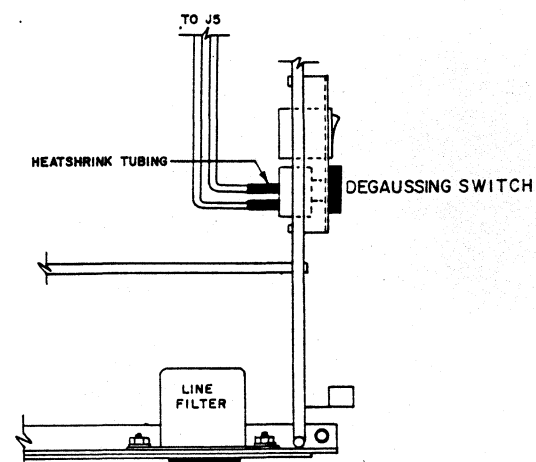
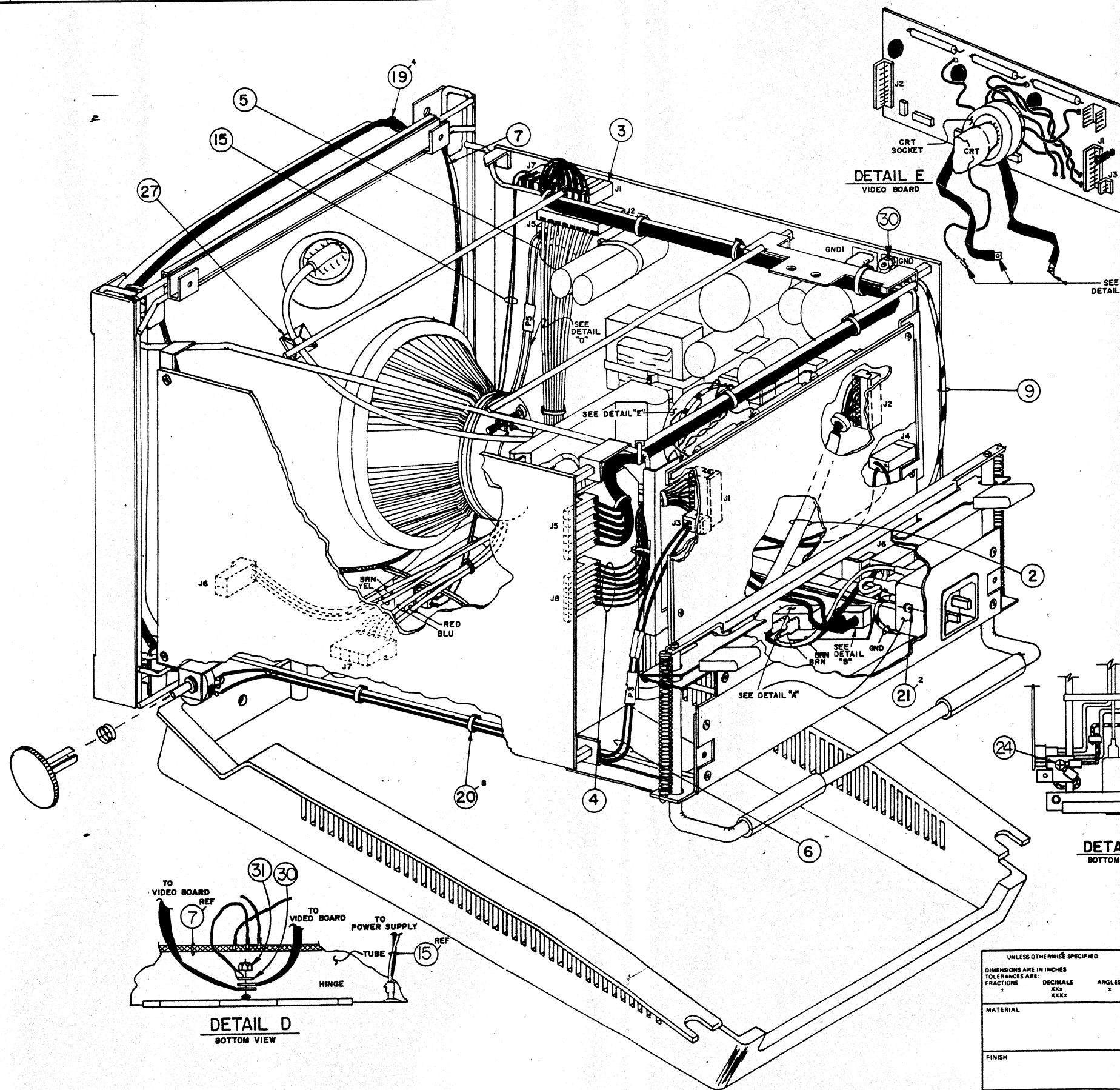
REV.	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4304	7/22/86	(Signature)
2	SEE ECN	4480, 4502, 4507, 4535	11/17/86	C.M.
3	SEE ECN	4607	12/10/86	C.M.
4	SEE ECN	4655	02/25/87	C.M.
5	SEE ECN	5048	6/28/87	J.C.



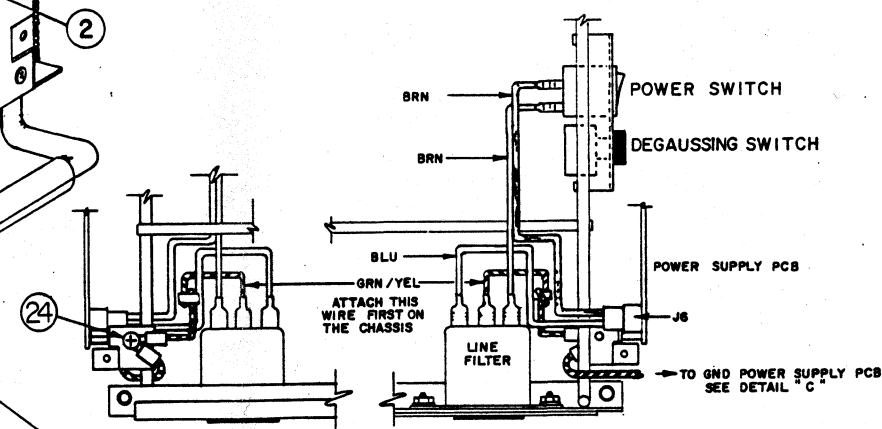
⚠ UNIT MUST BE BURNED IN, TESTED, AND SHIPPED WITH THE SAME LINE CORD.
NOTES:

DESIGNED BY: <i>SM</i> CHECKED: <i>C.M.</i> DATE: 7/22/86		APPROVED: <i>(Signature)</i> DATE: 7/22/86	
DRAWN: <i>SM</i> DATE: 7/22/86		INTENCOLOR TOP ASSEMBLY MONITOR MTR-3	
SIZE: D		DRAWING NO: 105466	
REV: 5		SHEET 1 OF 3	

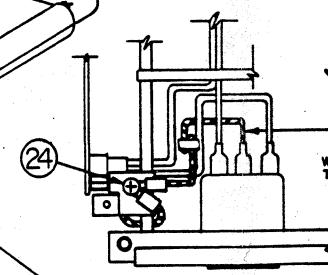
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4304	7/22/86	(Signature)
2	SEE ECN	4480, 4502, 4507, 4535	11/17/86	C.M.
3	SEE ECN	4607	12/10/86	C.M.
4	SEE ECN	4655	02/25/87	C.M.
5	SEE ECN	5049	6/28/89	J.C.



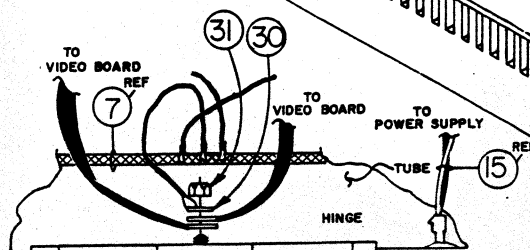
DETAIL B
TOP VIEW



DETAIL A
TOP VIEW



DETAIL C
BOTTOM VIEW



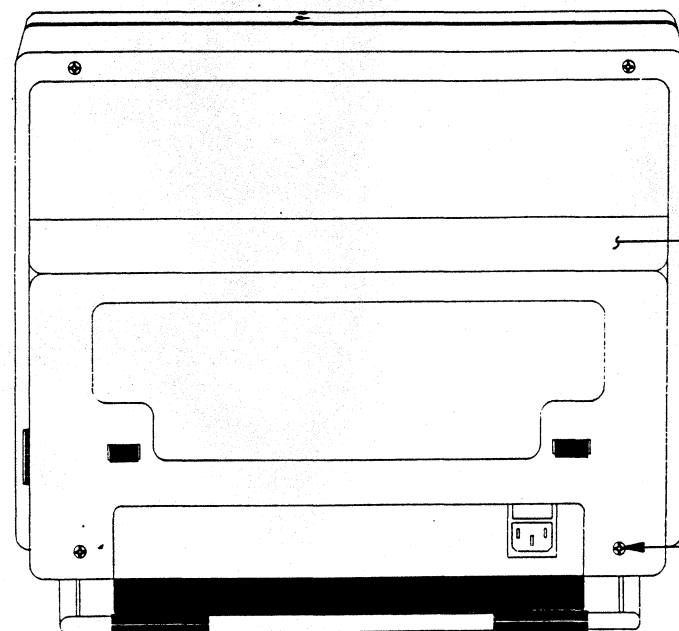
DETAIL D
BOTTOM VIEW

UNLESS OTHERWISE SPECIFIED			APPROVALS		DATE	
DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS			DRAWN	<i>[Signature]</i>	7/22/86	
			CHECKED	<i>[Signature]</i>	07/21/86	
			ENG	<i>[Signature]</i>	7/22/86	
MATERIAL			PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems.			
FINISH						
DO NOT SCALE DRAWING			SIZE D		DRAWING NO. 105466	REV 5
			SCALE		SHEET 2 OF 3	

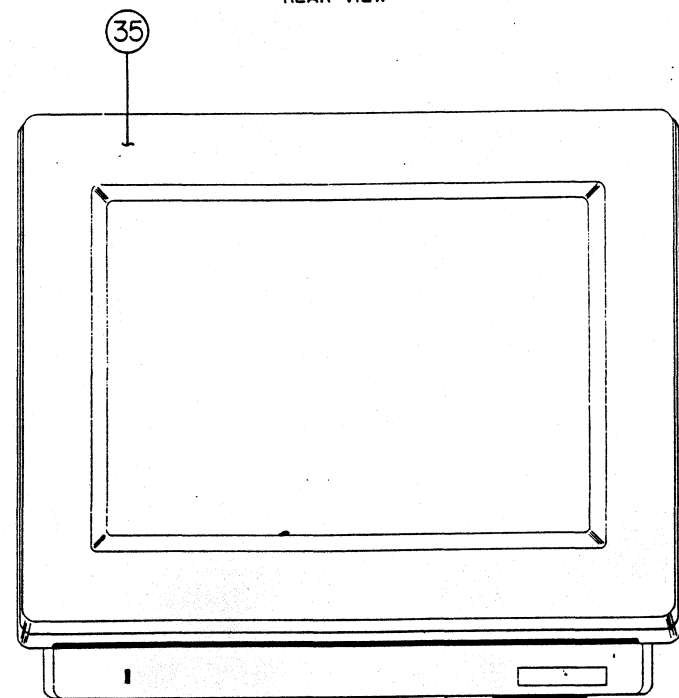


TOP ASSEMBLY MONITOR MTR-3

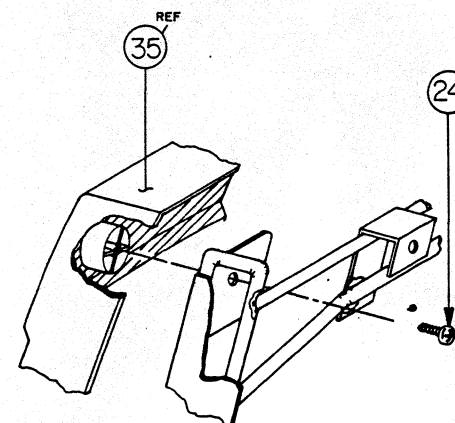
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4304	7/12/86	(Signature)
2	SEE ECN 4480, 4502, 4507, 4535		11/19/86	C.M.
3	SEE ECN 4607		12/10/86	C.M.
4	SEE ECN 4655		02/25/87	C.M.
5	SEE ECN 5049		6/29/88	J.E.



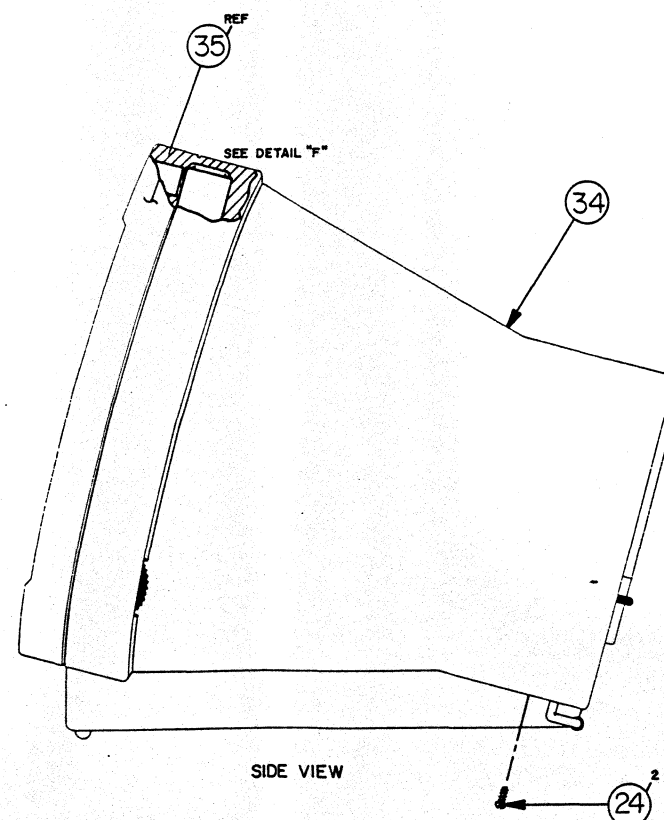
REAR VIEW



FRONT VIEW



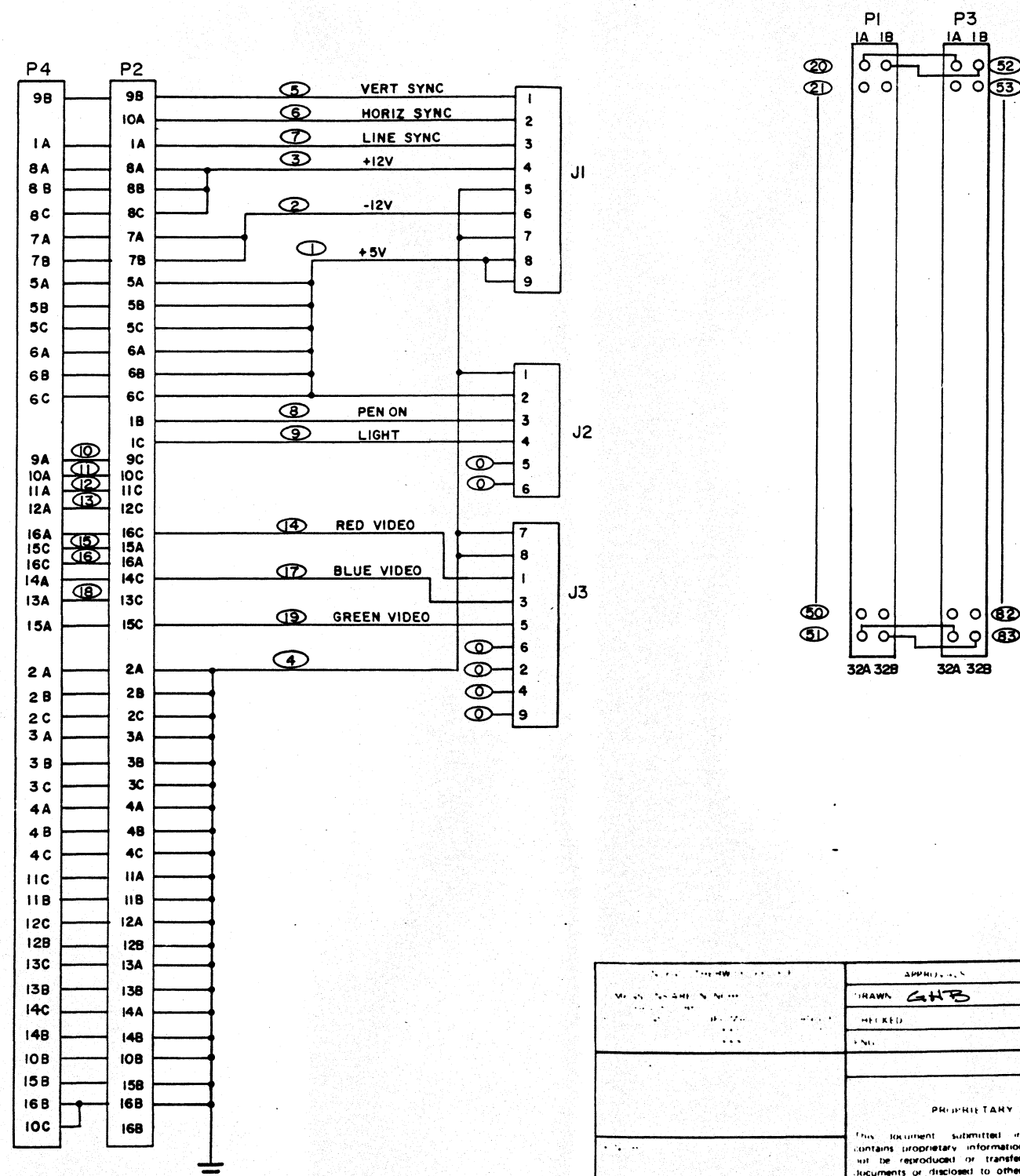
DETAIL F
BEZEL MOUNTING



SIDE VIEW

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	Intecolor	
DIMENSIONS ARE IN INCHES		DRAWN JERRY M. FORSH		7/8/86	TOP ASSEMBLY MONITOR MTR-3	
TOLERANCES ARE:		CHECKED C. Mott		7/12/86		
FRACTIONS DECIMALS ANGLES		ENG. P. Miller		7/27/86		
MATERIAL		PROPRIETARY		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems.		
FINISH		SIZE D		DRAWING NO. 105466		REV 5
DO NOT SCALE DRAWING		SCALE		SHEET 3 OF 3		

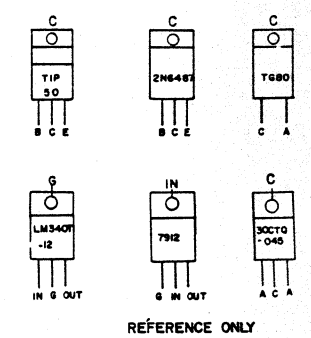
REVISIONS			
REV	DESCRIPTION	ECN	APPROVED DATE
1	ENG. RELEASE	4307	MAH 9/23/86



LEGEND
○ = INDICATES NODE NO

APPROVED DRAWN: GHB CHECKED: DATE: 7-18-86		Intecolor AN INTELLIGENT SYSTEMS COMPANY	
PROPRIETARY This document submitted in confidence contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems		SCHEMATIC AR-2 MOTHER BOARD	
SIZE C	DRAWING NO 105472	REV 1	SCALE NTS
SHEET 1 OF 1			

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
2	ENG RELEASE	3990	10/19/86	(Signature)
3	SEE ECN	4566	01/28/87	C.M.



- 9 DIRECTION OF ROTATION SHOW IS SPECIFIED WHEN ADJUSTING FROM BACK OF THE PCB.
- 8 FUTURE USE ONLY. NOT INSTALLED.
- 7 NOT AVAILABLE IN SOME CONFIGURATIONS.
- 6 ADJUST +5V WHILE MONITORING +5V TP ON LOGIC BD.
- 5 NODE REFERENCE NUMBERS ARE FOR CAD SYSTEM ROUTING. ZERO OHM RESISTORS ARE REQUIRED FOR NORMAL OPERATION.
- 4 PROPER OPERATION CAN ONLY BE GUARANTEED WITH USE OF INDICATED PARTS.
- 3 REMOVE W1 TO CHECK FREE-RUNNING FREQUENCY.
- 2 SEE TABLE 1 FOR CONFIGURATION.
- 1 FOR CONTINUED PROTECTION AGAINST FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE.

NOTES:

W4A	W4A	W4B	W4C	W4
W3B	W3A	W3C	W3C	W3
W1	W1	W1	W1	W1
KM-3TG	KM-3T	KM-3S	KM-3R	
24 KHZ	24 KHZ	18 KHZ	18 KHZ	

TABLE 1



SCHEMATIC KM-3 POWER SUPPLY

PATENT PENDING

APPROVALS	DATE
DRAWN DK MOORE	10-23-86
CHECKED C. M. Moore	10/19/86
ENG P. Moore	10/19/86

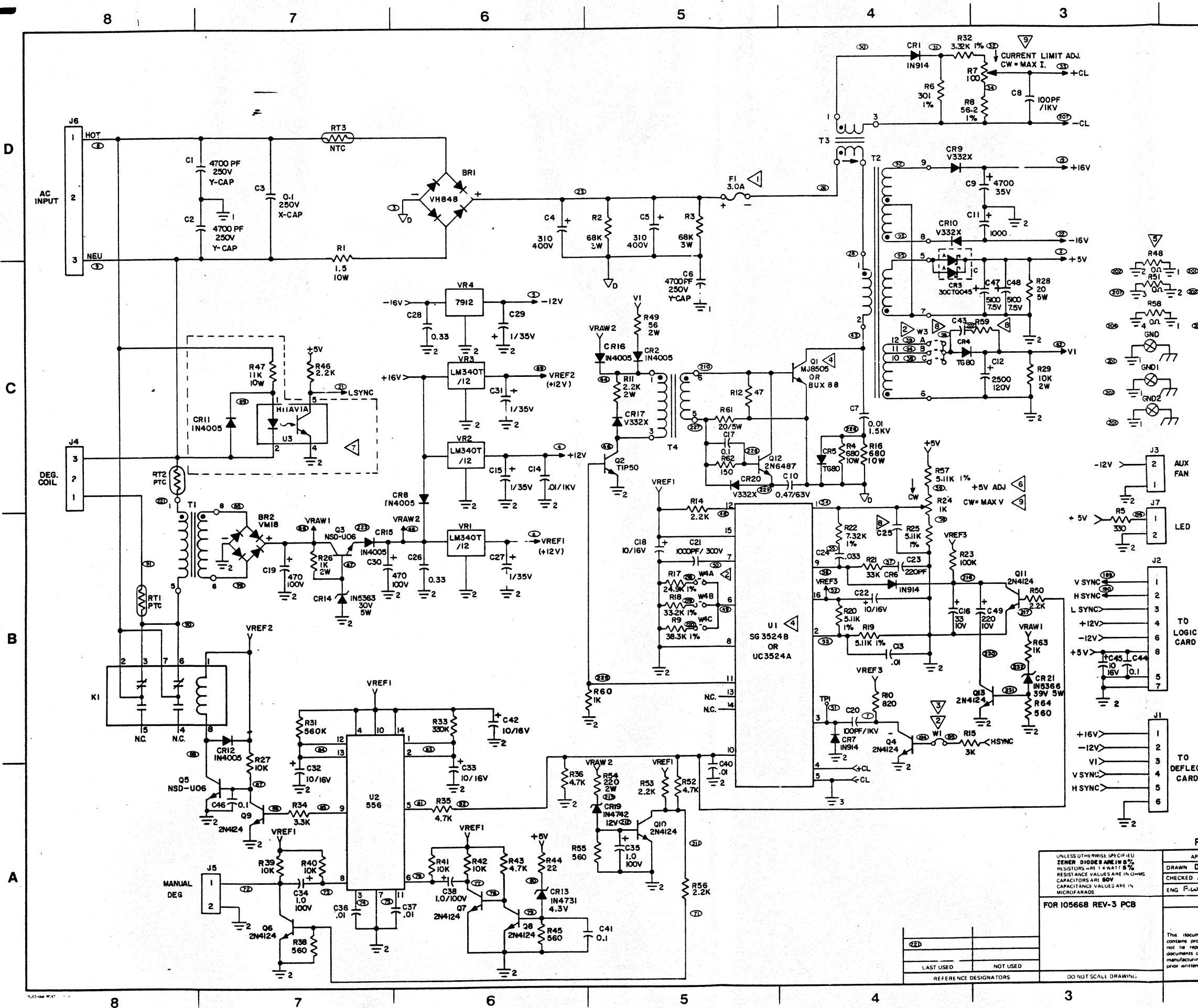
PROPRIETARY
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SIZE	DRAWING NO	REV
D	105667	3

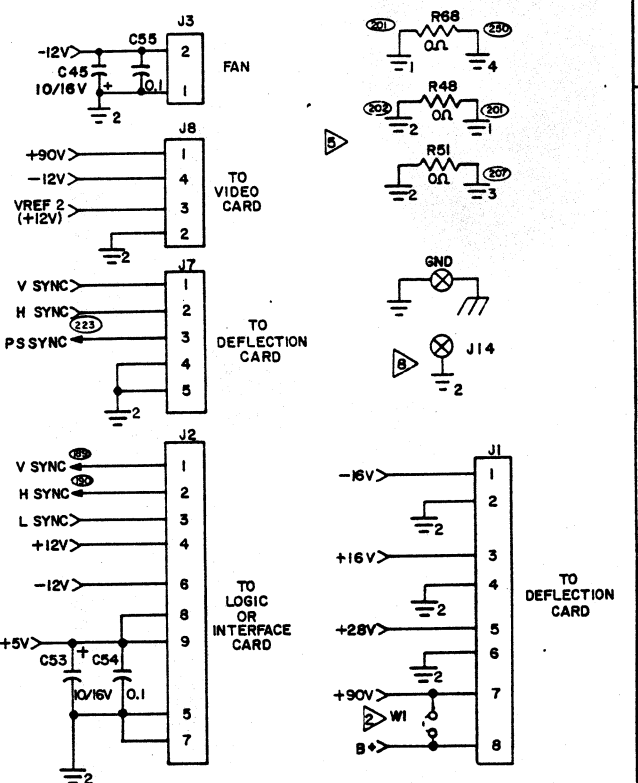
UNLESS OTHERWISE SPECIFIED:
ZENER DIODES ARE 1W 5%
RESISTORS ARE 1/4W 1% 0603
RESISTANCE VALUES ARE IN OHMS
CAPACITORS ARE 50V
CAPACITANCE VALUES ARE IN MICROFARADS

FOR 105668 REV-3 PCB

LAST USED	NOT USED
REFERENCE DESIGNATORS	DO NOT SCALE DRAWING



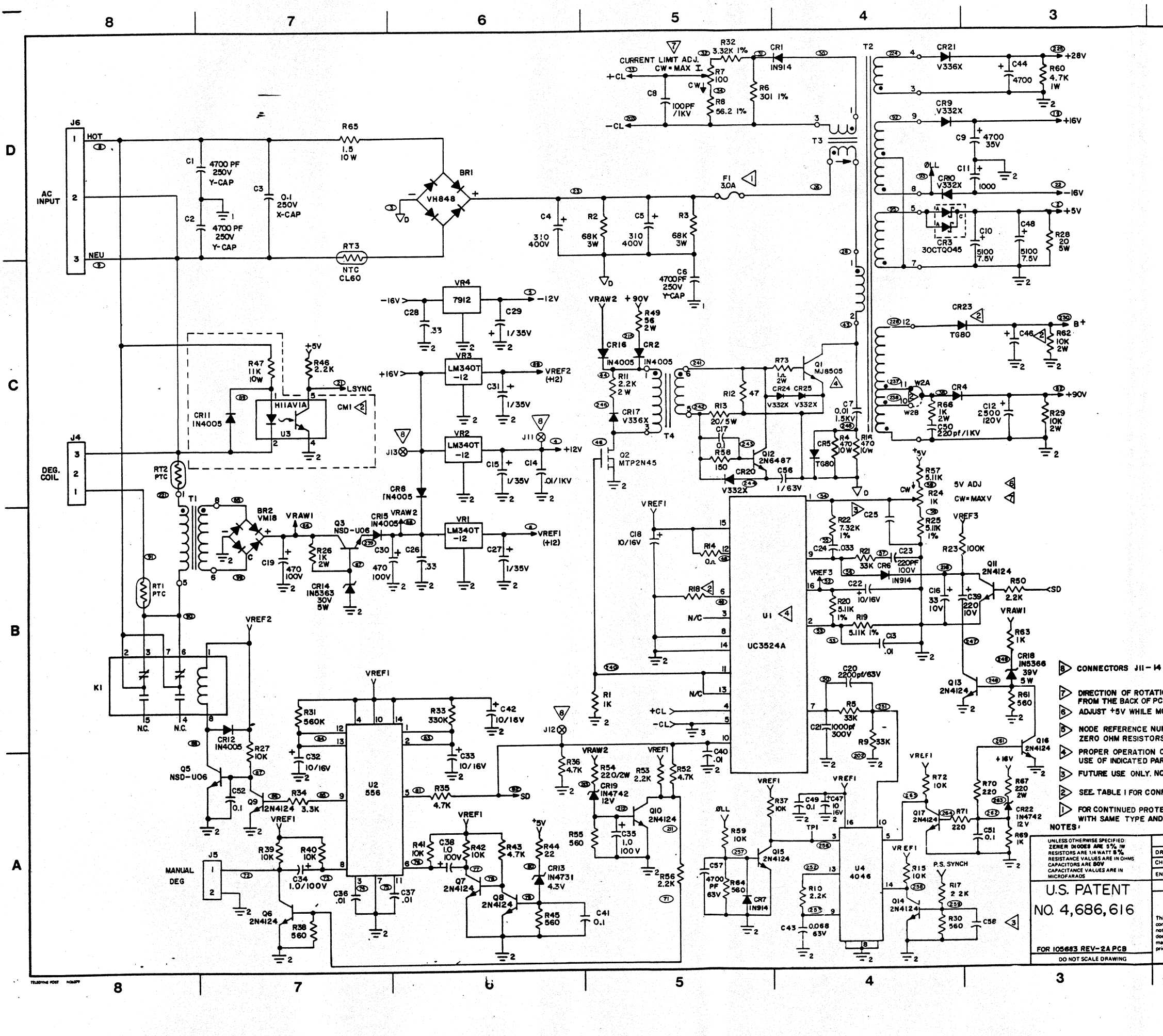
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4246	1/24/87	
2	SEE ECN	4815, 4730	4/20/87	J.L.
3	SEE ECN	4858	10/2/87	J.L.
4	SEE ECN	4892	12/15/87	J.L.



CONNECTORS J11-14 FOR OPTIONS ONLY.			
J11	TO VIDEO CARD	J12	TO DEFLECTION CARD
J13	TO LOGIC OR INTERFACE CARD	J14	TO DEFLECTION CARD

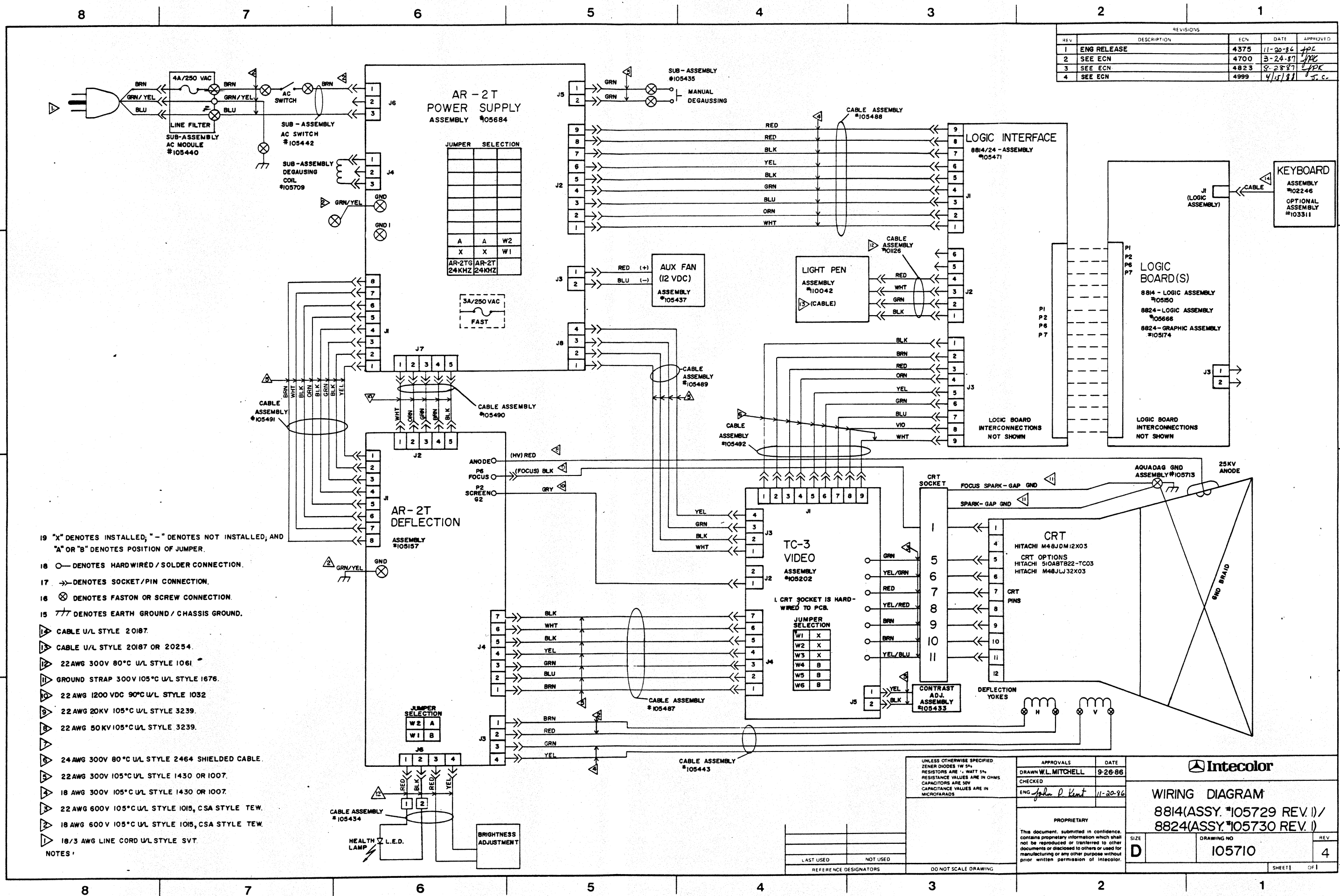
TABLE 1			
1900	2500	C46	
X		CR23	
19.6K	22.1K	R18	
	X	CM1	
A	A	W2	
	X	W1	
AR-2U	AR-2T		
30.5KHz	24 KHz		

U.S. PATENT NO. 4,686,616			
FOR 105683 REV-2A PCB	DO NOT SCALE DRAWING	DATE	12/11/85
APPROVALS	CHECKED	ENG	1/24/87
PROPRIETARY			
This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			
SIZE	D	DRAWING NO.	105682
REV	4	SHEET	1 OF 1



NOTES:			
1	UNLESS OTHERWISE SPECIFIED: ZENER DIODES ARE 5% IN RESISTORS ARE 1/4 WATT 5% RESISTANCE VALUES ARE IN OHMS CAPACITANCE VALUES ARE IN MICROFARADS		
2	DIRECTION OF ROTATION IS SPECIFIED WHEN ADJUSTING FROM THE BACK OF PCB.		
3	ADJUST +5V WHILE MONITORING +5V TP ON LOGIC BOARD.		
4	NODE REFERENCE NUMBER ARE CAD SYSTEM ROUTING. ZERO OHM RESISTORS ARE REQUIRED FOR NORMAL OPERATION.		
5	PROPER OPERATION CAN ONLY BE GUARANTEED WITH USE OF INDICATED PARTS.		
6	FUTURE USE ONLY. NOT INSTALLED.		
7	SEE TABLE 1 FOR CONFIGURATION ("X"=INSTALLED "-"=NOT)		
8	FOR CONTINUED PROTECTION AGAINST FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE.		

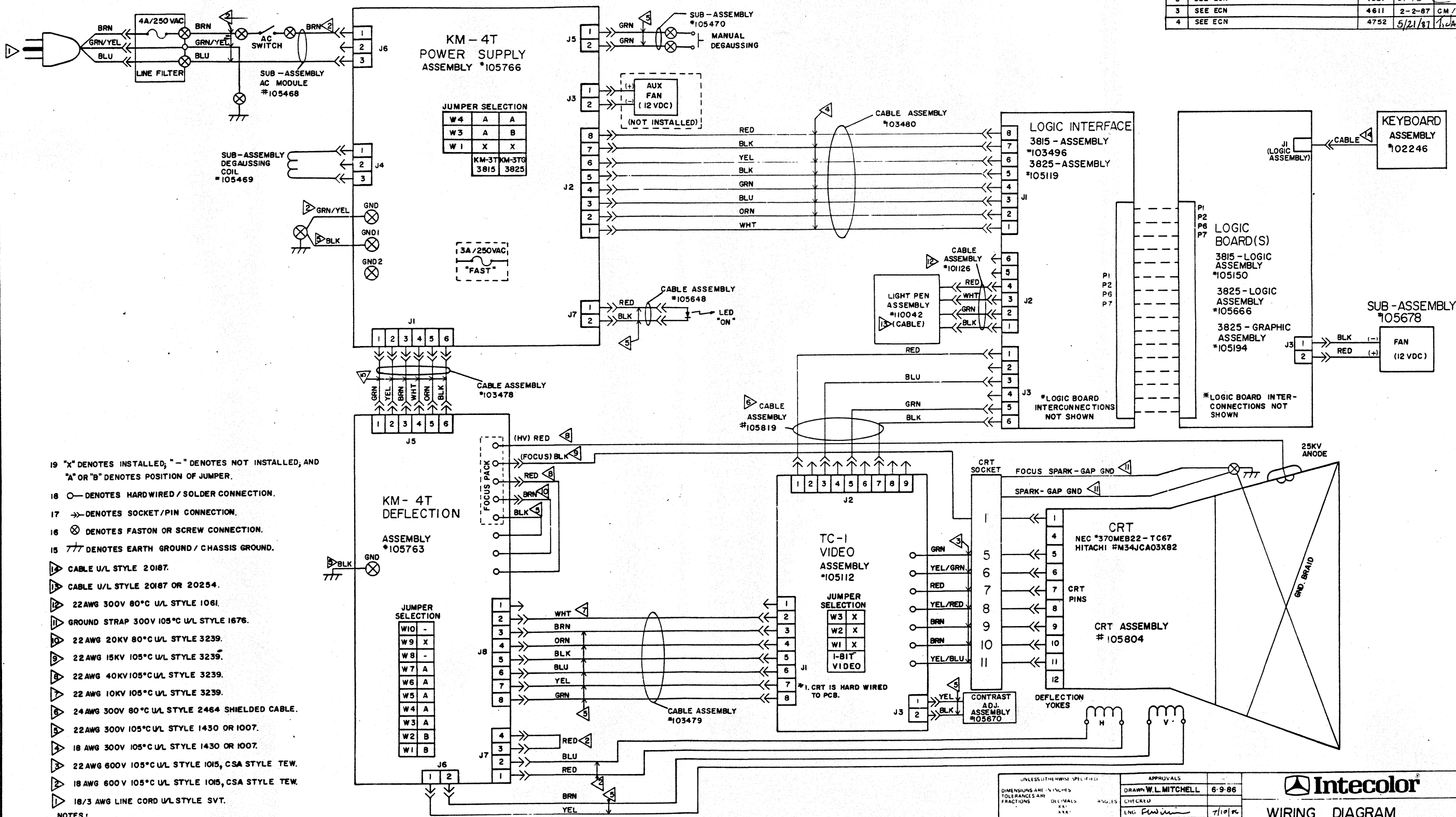
Intecolor			
SCHEMATIC AR-2 POWER SUPPLY			



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4375	11-20-84	JPL
2	SEE ECN	4700	3-24-87	JPL
3	SEE ECN	4823	8-28-87	JPL
4	SEE ECN	4999	4/15/91	J.C.

APPROVALS		DATE		WIRING DIAGRAM 8814(ASSY. *105729 REV. I) / 8824(ASSY. *105730 REV. I)
DRAWN W.L. MITCHELL		9-28-86		
CHECKED				
ENG John P Kent		11-20-96		
PROPRIETARY				
This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			SIZE	DRAWING NO
			D	105710
				REV
				4
			SHEET 1 OF 1	

REV	DESCRIPTION	DATE	BY
1	ENG. RELEASE	4412	7/10/86
2	SEE ECN	4521	12/7/84
3	SEE ECN	4611	2-2-87 CM/JC
4	SEE ECN	4752	5/21/87

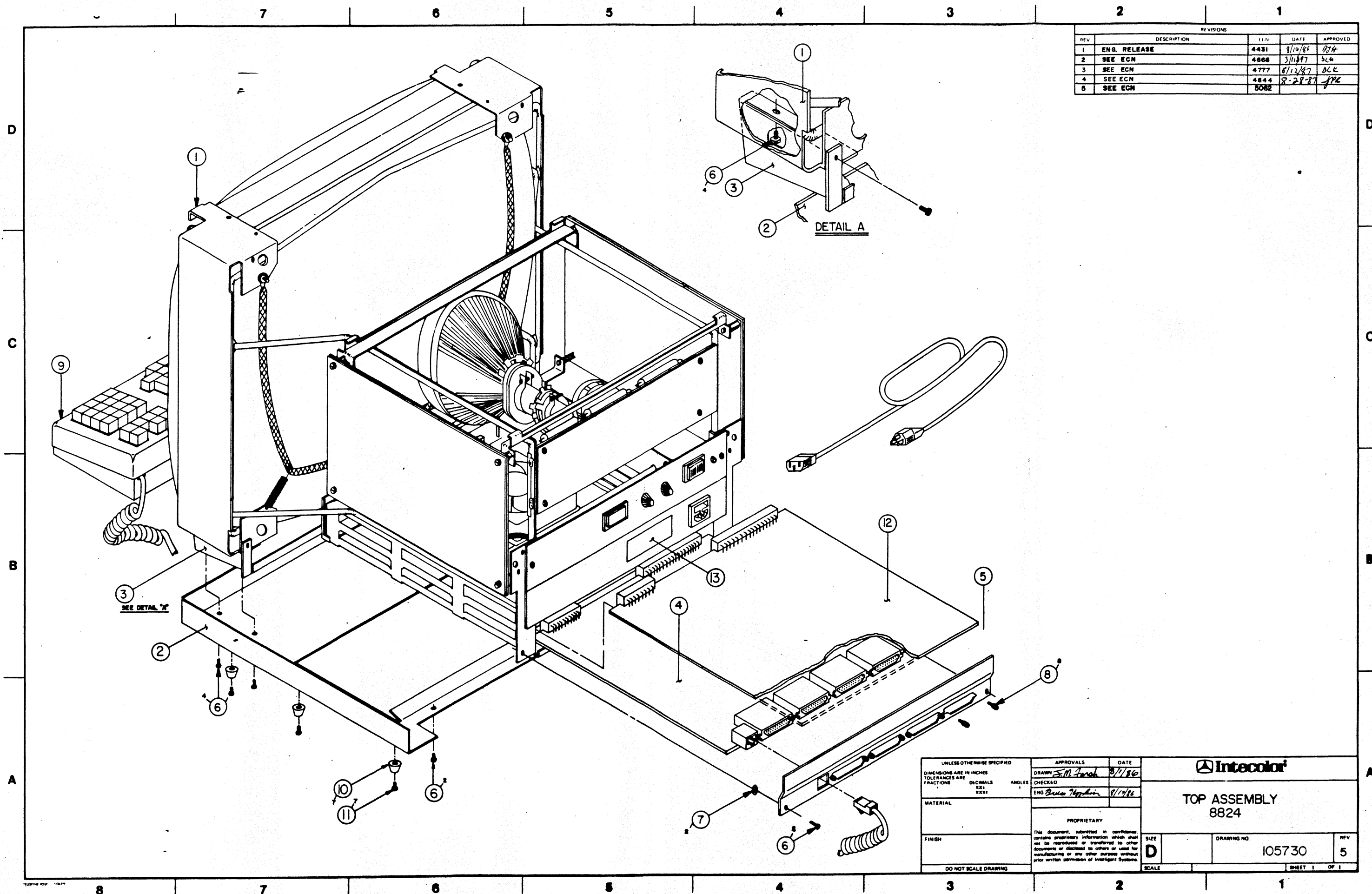


UNLESS OTHERWISE SPECIFIED		APPROVALS	
DIMENSIONS ARE IN INCHES	DECIMALS	DRAWN W.L. MITCHELL	6-9-86
TOLERANCES ARE FRACTIONS	ANGLES	CHECKED	
		ENG. <i>Fin</i>	7/10/86
MATERIAL		PROPRIETARY	
FINISH		This document submitted in confidence contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without written permission of Intecolor Systems.	
DO NOT SCALE DRAWING		SIZE	D
		DRAWING NO	105720
		REV	4

Intecolor

WIRING DIAGRAM
3815 (ASSY #105444 REV. 3) /
3825 (ASSY #105446 REV. 3)

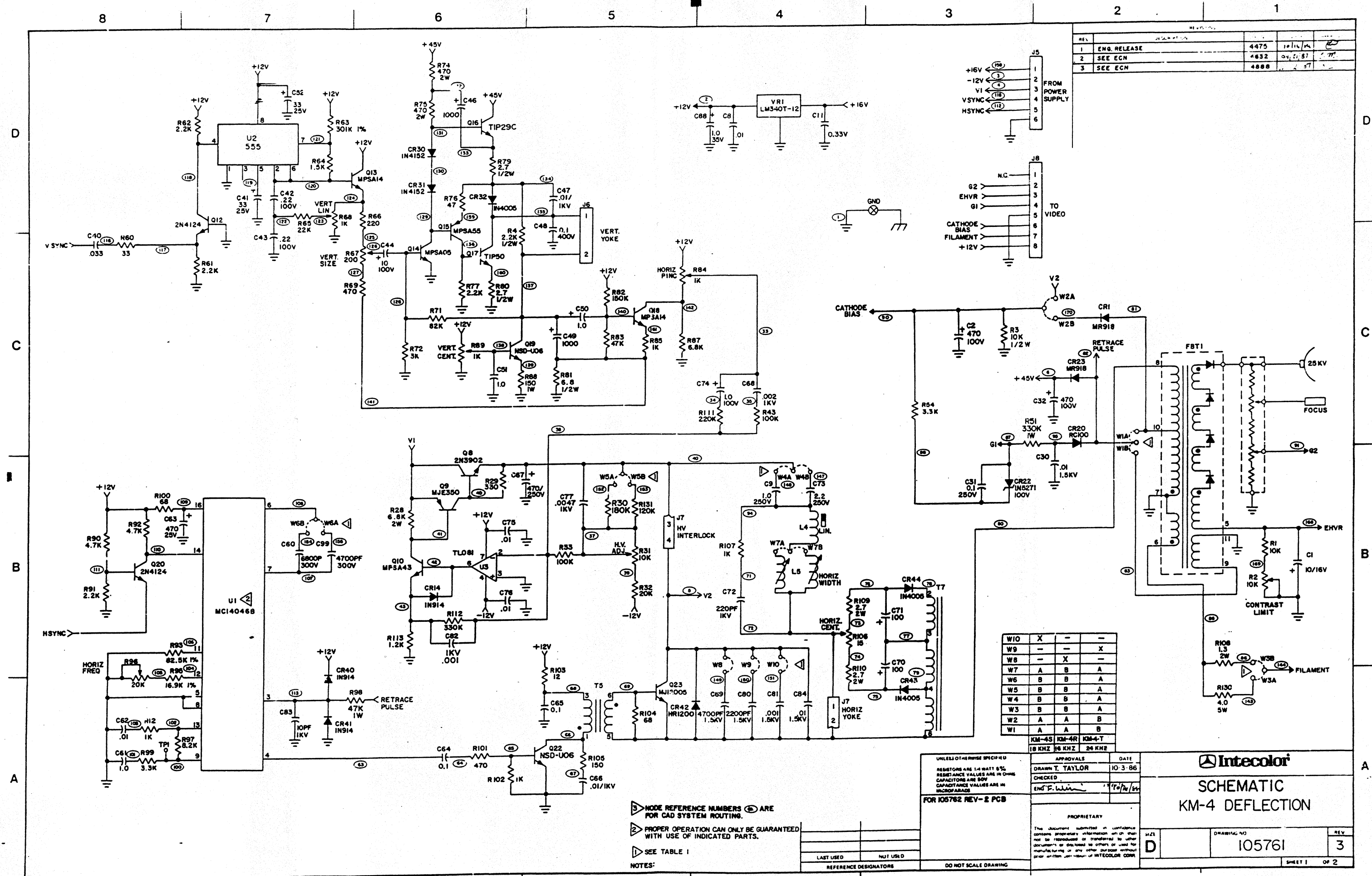
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4431	8/14/86	BJS
2	SEE ECN	4668	3/11/87	SCW
3	SEE ECN	4777	6/12/87	BLK
4	SEE ECN	4844	8-28-87	JPL
5	SEE ECN	5082		

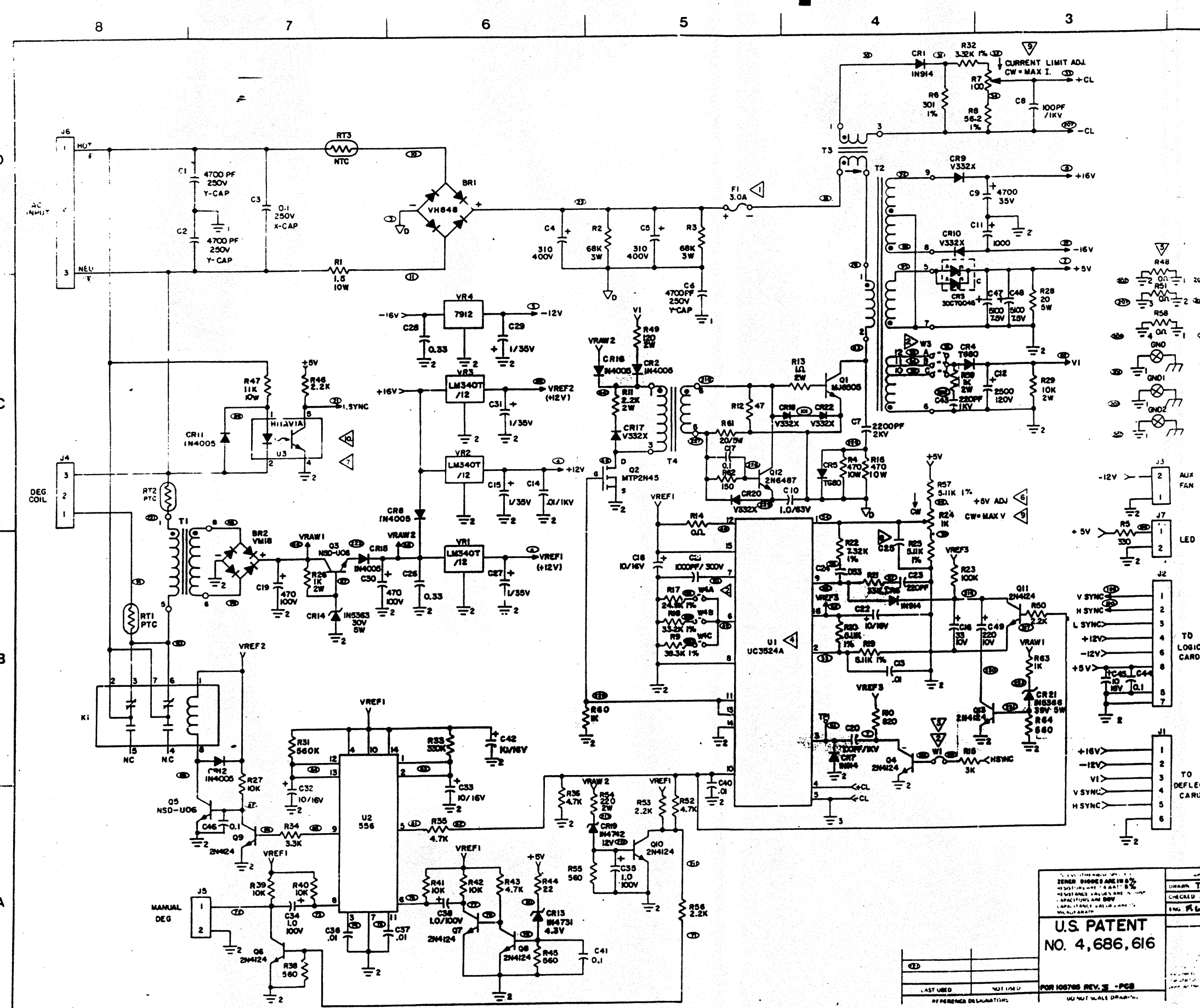


UNLESS OTHERWISE SPECIFIED			APPROVALS		DATE				
DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS	DECIMALS XXX XXX	ANGLES °	DRAWN	<i>S.M. Smith</i>	<i>8/1/86</i>	TOP ASSEMBLY 8824			
			CHECKED						
			ENG	<i>Bruce Thompson</i>	<i>8/14/86</i>				
MATERIAL		PROPRIETARY				SIZE			
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor Systems.							
DO NOT SCALE DRAWING		SCALE							
						DRAWING NO.		105730	REV
								SHEET 1	OF 1

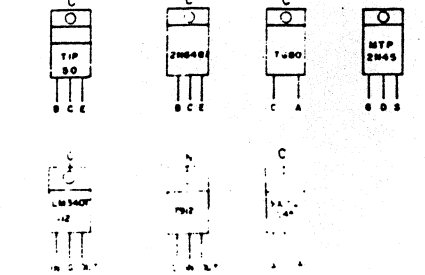
Intecolor
TOP ASSEMBLY
8824

SIZE	D	DRAWING NO.	105730	REV	5
SCALE		SHEET	1	OF	1





1	ENG RELEASE	4479	10/10/66	C.M.
2	SEE ECN	4611	01/25/67	C.M.
3	SEE ECN	4808	07/25/67	C.M.
4	SEE ECN	4858	10/3/67	J.L.
5	SEE ECN	4898	11/16/67	J.L.
6	SEE ECN	5019	4-2-68	J.M.



- 10 INSTALL FOR PHILLIPS MEDICAL.
- 9 DIRECTION OF ROTATION SHOWN IS SPECIFIED WHEN ADJUSTING FROM BACK OF THE PCB.
- 8 FUTURE USE ONLY NOT INSTALLED.
- 7 USED ON LINE-LOCKED MODELS ONLY.
- 6 ADJUST -5V WHILE MONITORING -5V TP ON LOGIC BD.
- 5 NODE REFERENCE NUMBERS ARE FOR CAD SYSTEM ROUTING. ZERO OHM RESISTORS ARE REQUIRED FOR NORMAL OPERATION.
- 4 PROPER OPERATION CAN ONLY BE GUARANTEED WITH USE OF INDICATED PARTS.
- 3 REMOVE W1 TO CHECK FREE-RUNNING FREQUENCY.
- 2 SEE TABLE 1 FOR CONFIGURATION.
- 1 FOR CONTINUED PROTECTION AGAINST FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE.

NOTES

W4A	W4A	W4B	W4C	W4
W3B	W3A	W3C	W3C	W3
W1	W1	W1	W1	W1
KM-3T6	KM-3T	KM-3S	KM-3R	
24 KHZ	24 KHZ	16 KHZ	16 KHZ	

TABLE 1

U.S. PATENT NO. 4,686,616

FOR 105766 REV. 3 - PCB

DESIGNER: TAYLOR

CHECKED: C. M. J.

ENG: R. J. J.

10-3-66

10/16/66

Intecolor

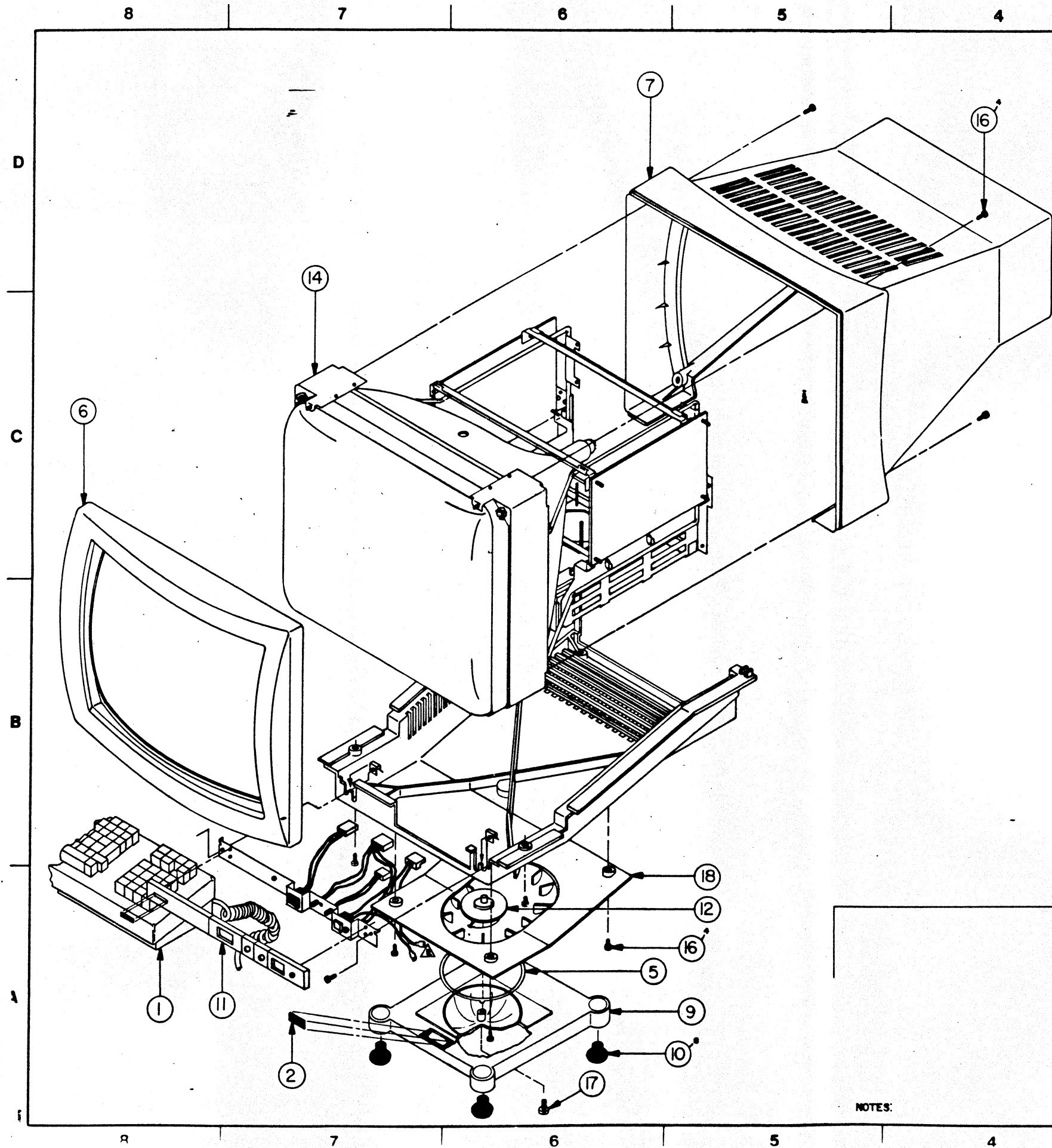
SCHEMATIC

KM-4 POWER SUPPLY

D

105764

6

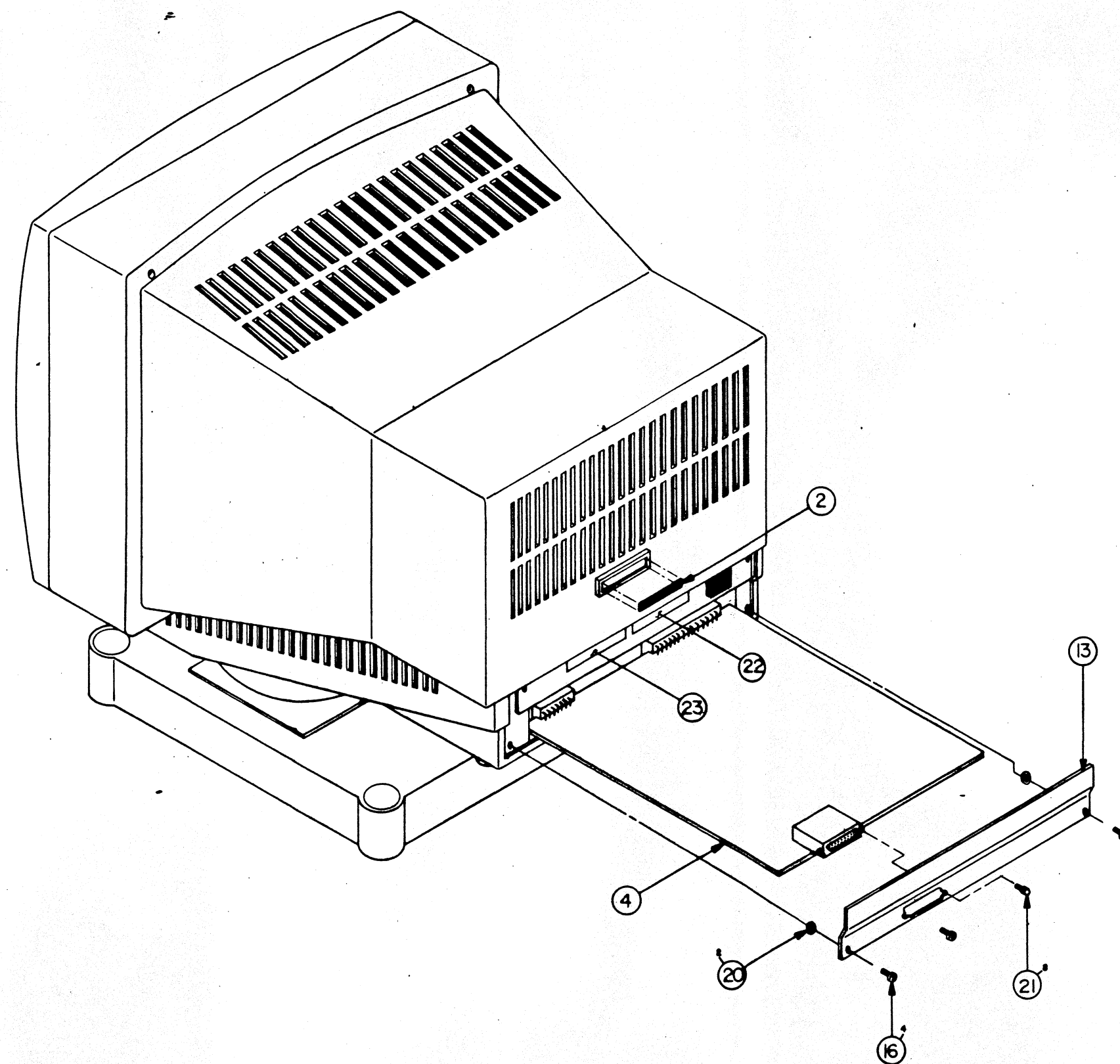


REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4623	11/3/86	B.L.H.
2	SEE ECN	4657, 4666, 4668	3/11/87	B.L.H.
3	SEE ECN	4692	3/22/87	S.C.
4	SEE ECN	4777	6/1/87	J.L.H.
5	SEE ECN	4787	6/28/87	J.L.H.
6	SEE ECN	4792	7/27/87	J.L.H.
7	SEE ECN	4845	8/21/87	J.L.H.

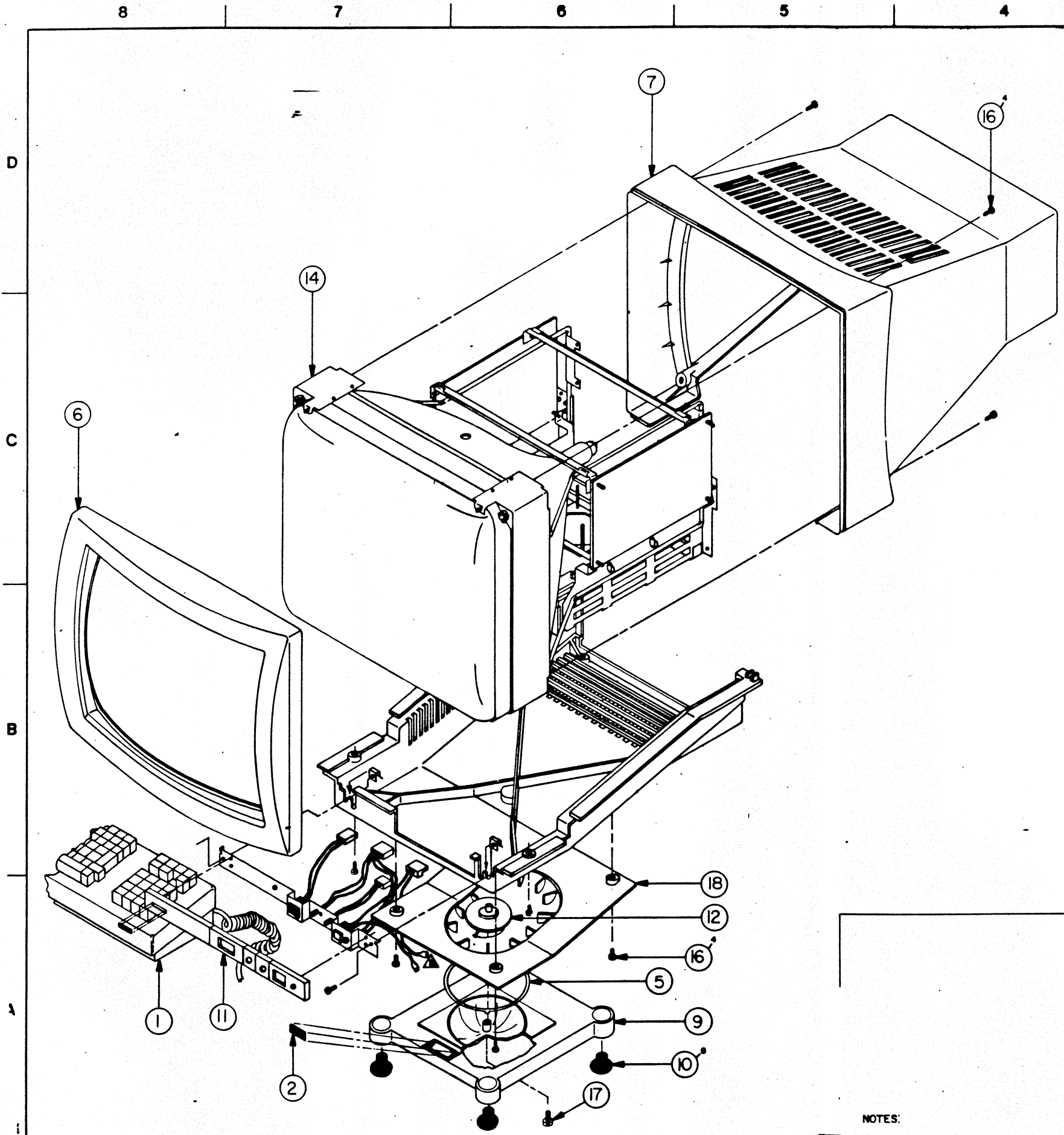
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MM (INCHES) TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 1/16 0.1 1/16 0.1 1/16 0.1		APPROVALS DRAWN <i>St. J. Smith</i> 11/3/86 CHECKED ENG <i>Steve Martin</i> 11/3/86		DATE 11/3/86	
MATERIAL		PROPRIETARY		Intecolor	
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		TOP ASSEMBLY 8815	
DO NOT SCALE DRAWING		SIZE D		DRAWING NO. 105904	
		SCALE		REV 7	

NOTES:

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4523	11/3/81	BCH
2	SEE ECN	4657, 4668, 4688	3/11/82	NLD
3	SEE ECN	4692	3/22/82	J.C.
4	SEE ECN	4777	6/10/82	BCH
5	SEE ECN	4727	6/15/82	J.C.
6	SEE ECN	4792	7/27/82	W.S.
7	SEE ECN	4846	8/11/82	APK



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE			
DIMENSIONS ARE IN MM (INCHES)		DRAWN <i>Sam M. Smith</i>		9/20/86		TOP ASSEMBLY 8815	
TOLERANCES ARE:		CHECKED <i>0</i>					
FRACTIONS	DECIMALS	ENG <i>Bruce Hopkins</i>		11/3/86			
1	.001						
ANGLES							
MATERIAL							
		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.					
FINISH				SIZE D		DRAWING NO. 105904	
						REV 7	
DO NOT SCALE DRAWINGS				SCALE		SHEET 1 OF 1	

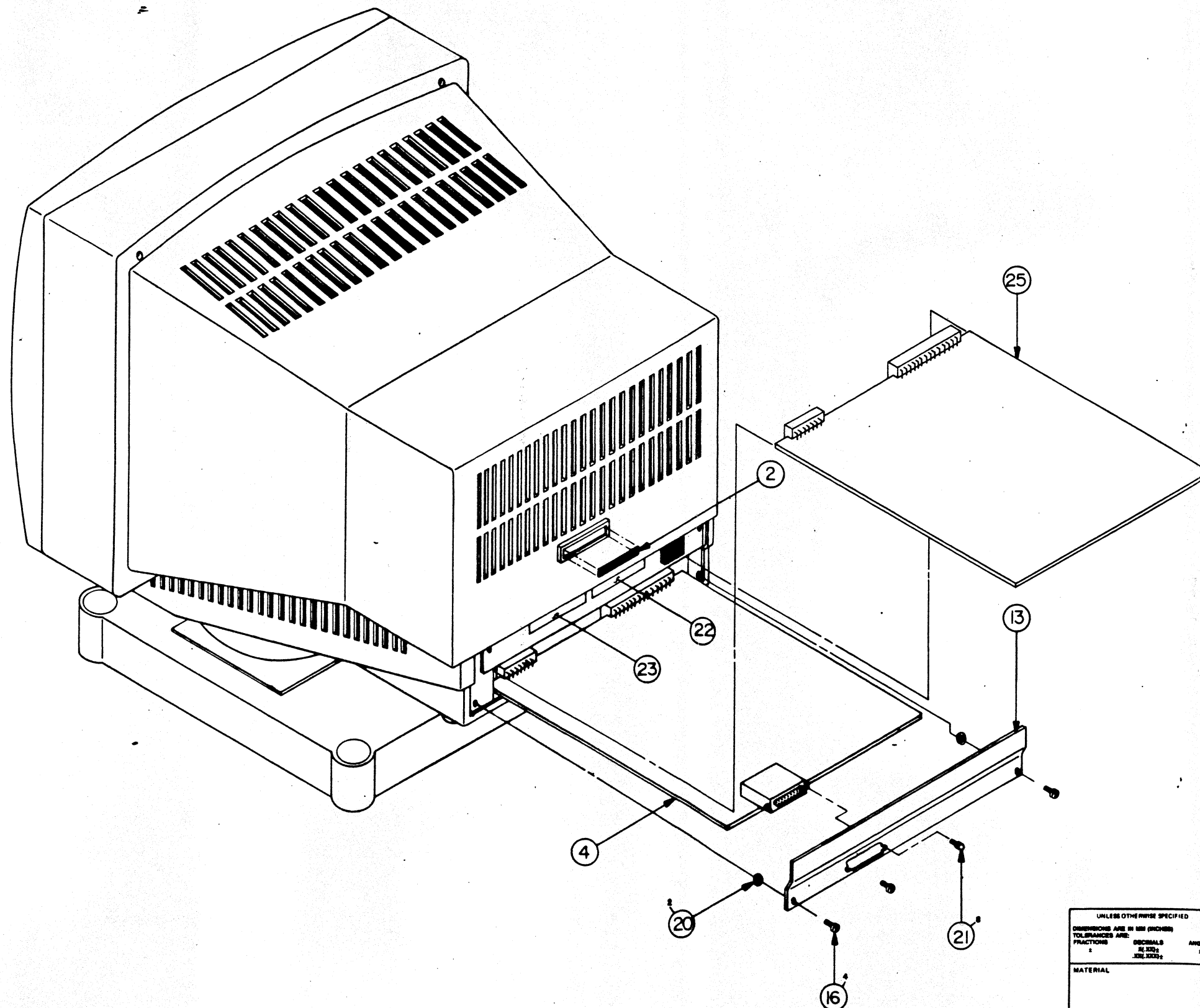


REVISIONS				
REV	DESCRIPTION			
1	ENG. RELEASE	4525	11/3/86	D.L.H.
2	SEE ECN	4657, 4668, 4688	3/11/87	Q.L.P.
3	SEE ECN	4692	3/25/87	J.C.
4	SEE ECN	4777	1/11/87	B.L.H.
5	SEE ECN	4727	6/25/87	J.L.
6	SEE ECN	4792	7/27/87	B.L.H.
7	SEE ECN	4848	8/21/87	J.P.K.
8	SEE ECN	4979	3/1/88	J.C.
9	SEE ECN	5062		

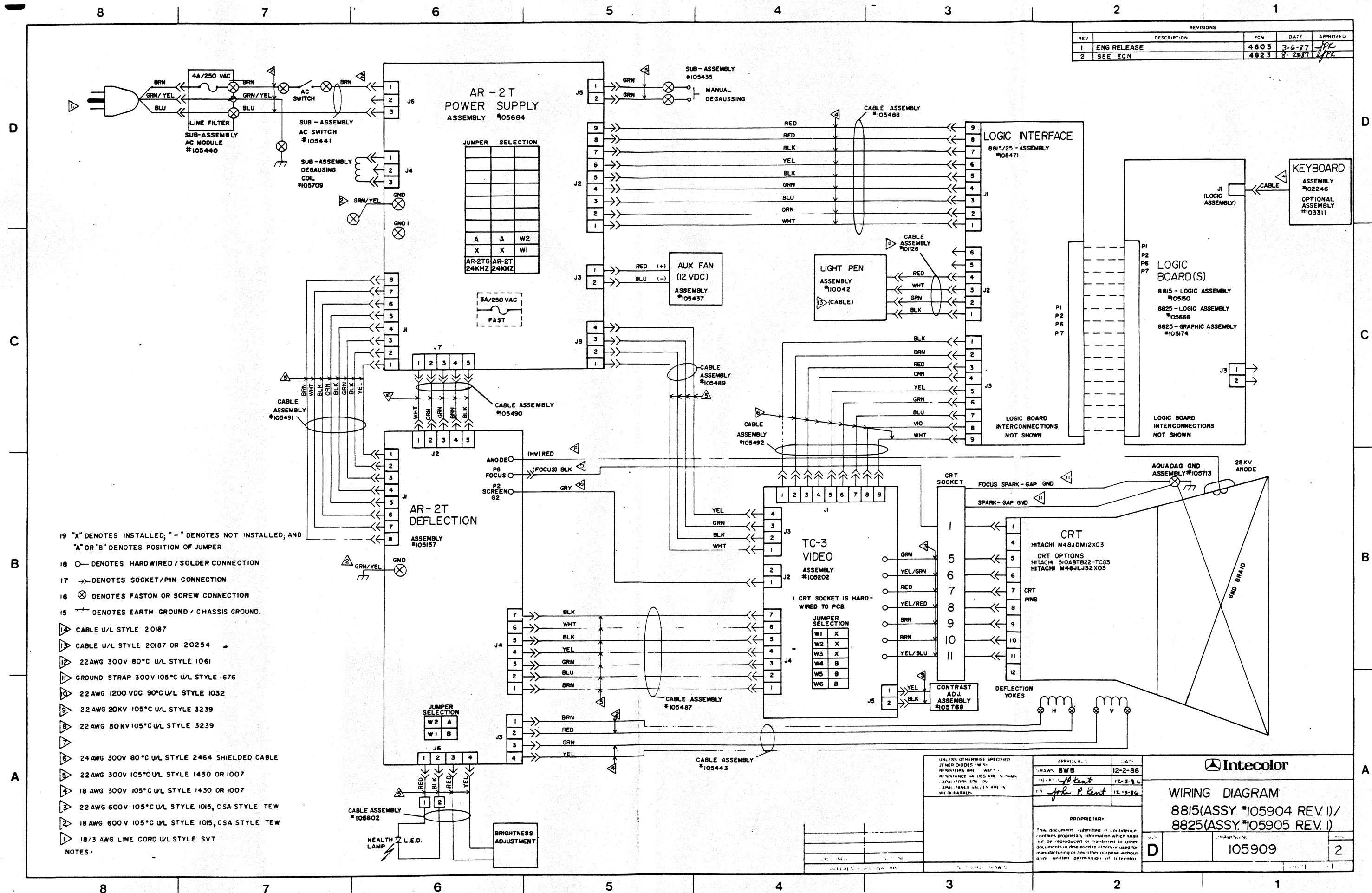
NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 1 10, 100, 1000		APPROVALS DRAWN <i>[Signature]</i> 11/3/86 CHECKED <i>[Signature]</i> ENG <i>[Signature]</i> 11/3/86	DATE 11/3/86		
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		TOP ASSEMBLY 8825	
FINISH		SIZE D		DRAWING NO. 105905	REV 9
DO NOT SCALE DRAWING		SCALE			

REVISIONS				
REV	DESCRIPTION	DATE	BY	APP
1	TRG. RELEASE	4623	11/3/66	
2	SEE ECH	4657,4668,4688	11/3/67	Q.H.
3	SEE ECH	4692	11/25/67	J.C.
4	SEE ECH			P.L.A.
5	SEE ECH			
6	SEE ECH			



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MM (INCHES) TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 1 0.1 0.1 0.1		APPROVALS DRAWN <i>Sam M. Smith</i> 9/10/66 CHECKED <i>Eng Bruce Hopkins</i> 11/3/66 DATE		DATE	
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		Intecolor TOP ASSEMBLY 8825	
FINISH		SIZE D		DRAWING NO. 105905	
DO NOT SCALE DRAWING		SCALE		REV 9	



8

7

6

5

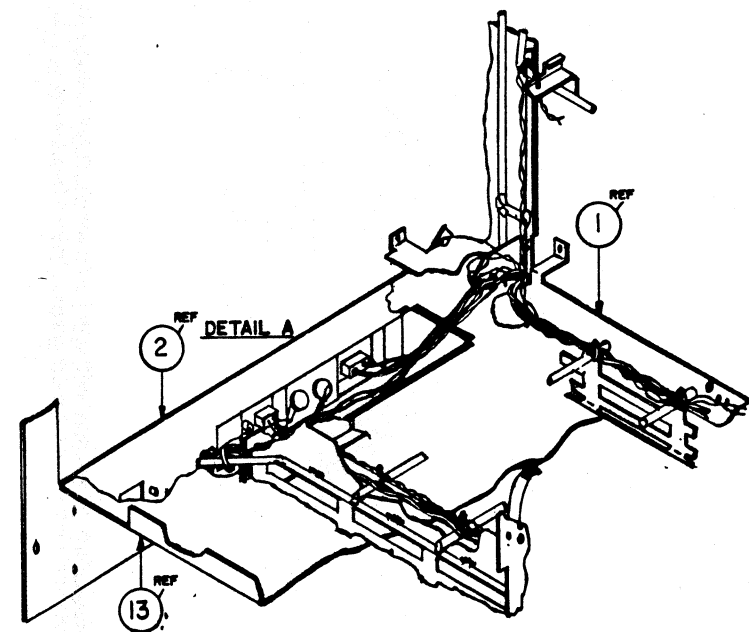
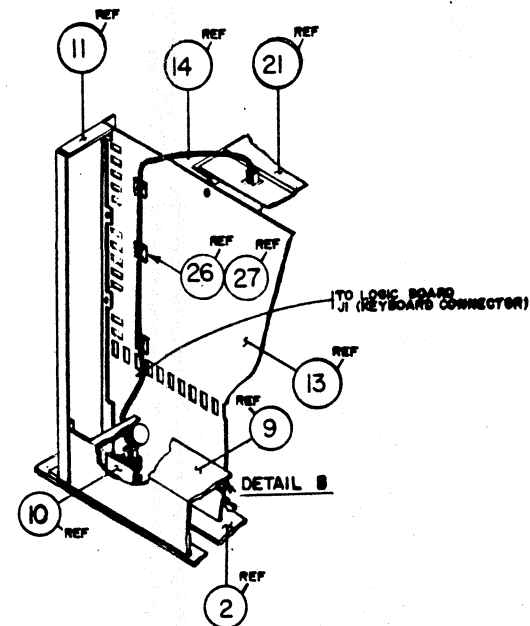
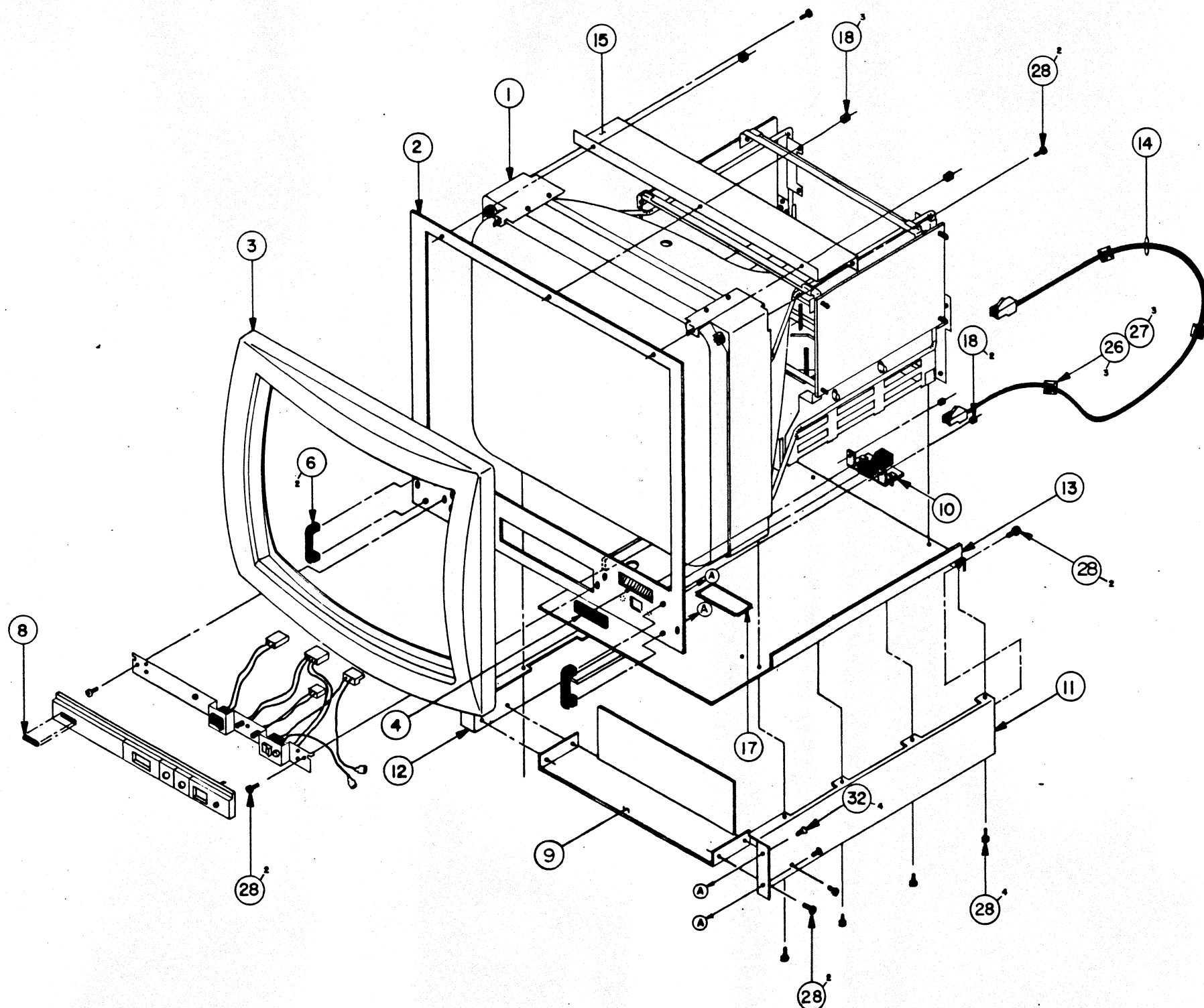
4

3

2

1

REV	DESCRIPTION	DATE	BY	CHKD
1	ENG. RELEASE	4677	1/10/87	DLA
2	SEE ECN	4662, 4666, 4668, 4672	3/10/87	DLA
3	SEE ECN	4692	3/25/87	JG
4	SEE ECN	4770, 4777	6/10/87	DLA
5	SEE ECN	4727	6/25/87	JG
6	SEE ECN	4792, 4800, 4801	7/27/87	DLA
7	SEE ECN	4866, 4872	9/15/87	DLA
8	SEE ECN	4988	3/10/89	h2H



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN MM (INCHES)		DRAWN <i>S.M. Forsh</i>		7/6/86	
TOLERANCES ARE:		CHECKED			
FRACTIONS		DECIMALS		ANGLES	
1/2, 3/4, 1, 1 1/2, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48, 60, 72, 96, 120, 144, 180, 216, 240, 288, 360		1/2, 3/4, 1, 1 1/2, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48, 60, 72, 96, 120, 144, 180, 216, 240, 288, 360		1/2, 3/4, 1, 1 1/2, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48, 60, 72, 96, 120, 144, 180, 216, 240, 288, 360	
MATERIAL		PROPRIETARY			
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purposes without prior written permission of Intecolor.			
DO NOT SCALE DRAWING		SIZE D		DRAWING NO. 105941	
		SCALE		SHEET 1 OF 2	

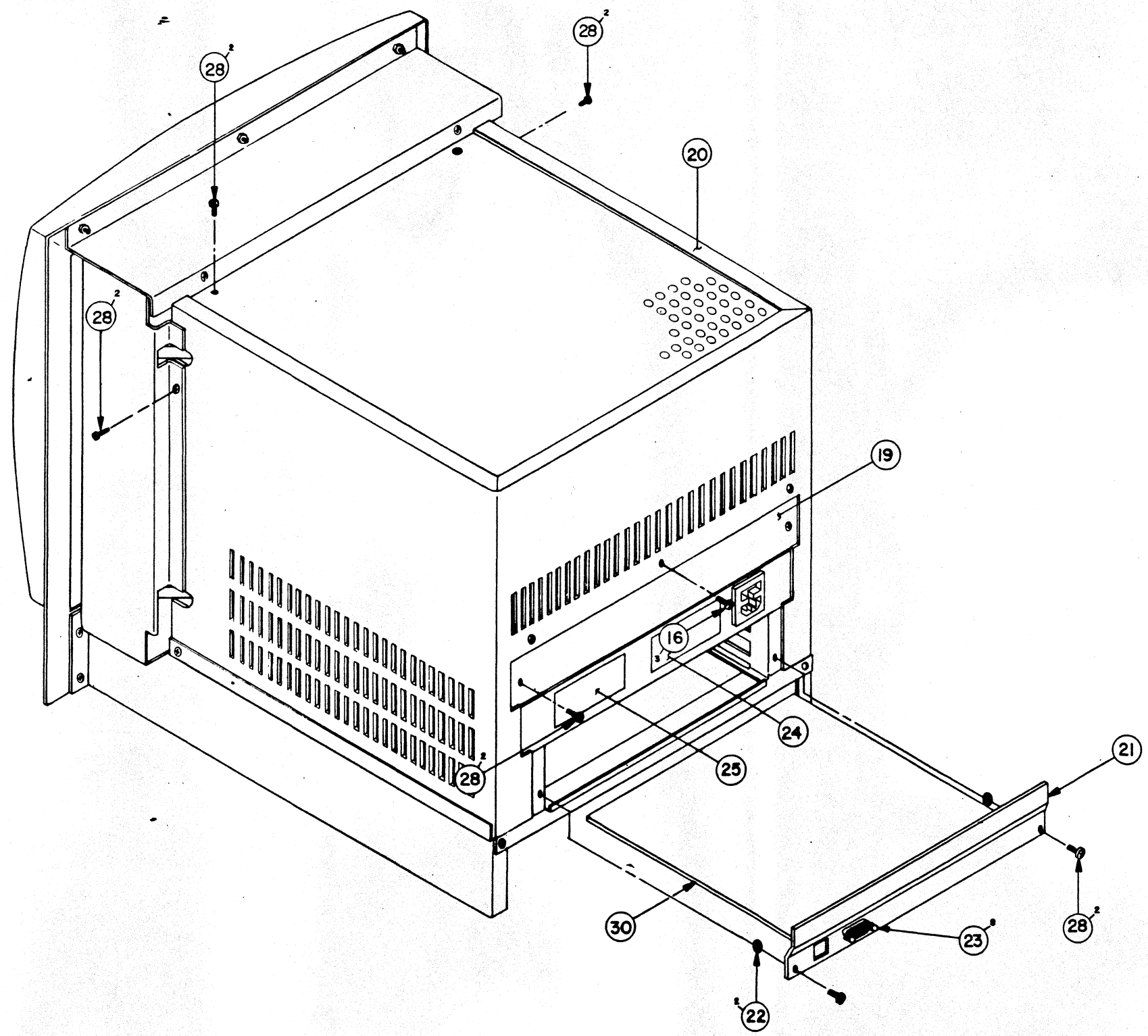
Intecolor

TOP ASSEMBLY 8865

REV 8

8 7 6 5 4 3 2 1

REVISIONS				
REV	DESCRIPTION	DATE	BY	CHK
1	ENG. RELEASE	4677	1/11/87	SLA
2	SEE ECN	4662, 4666, 4668, 4672	3/11/87	SLA
3	SEE ECN	4692	3/25/87	SLA
4	SEE ECN	4770, 4777	6/18/87	SLA
5	SEE ECN	4727	6/25/87	SLA
6	SEE ECN	4792, 4800, 4801	7/27/87	SLA
7	SEE ECN	4866, 4872	9/24/87	SLA
8	SEE ECN	4888	3/10/88	SLA



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN INCHES		DRAWN <i>S.M. Galt</i>		12/4/86	
TOLERANCES ARE:		CHECKED			
FRACTIONS 1/16, 1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8		ENG <i>John P. Galt</i>		1/10/87	
MATERIAL		PROPRIETARY			
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transmitted to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			
DO NOT SCALE DRAWING		SIZE D		DRAWING NO. 105941	
		SCALE		SHEET 2 OF 2	

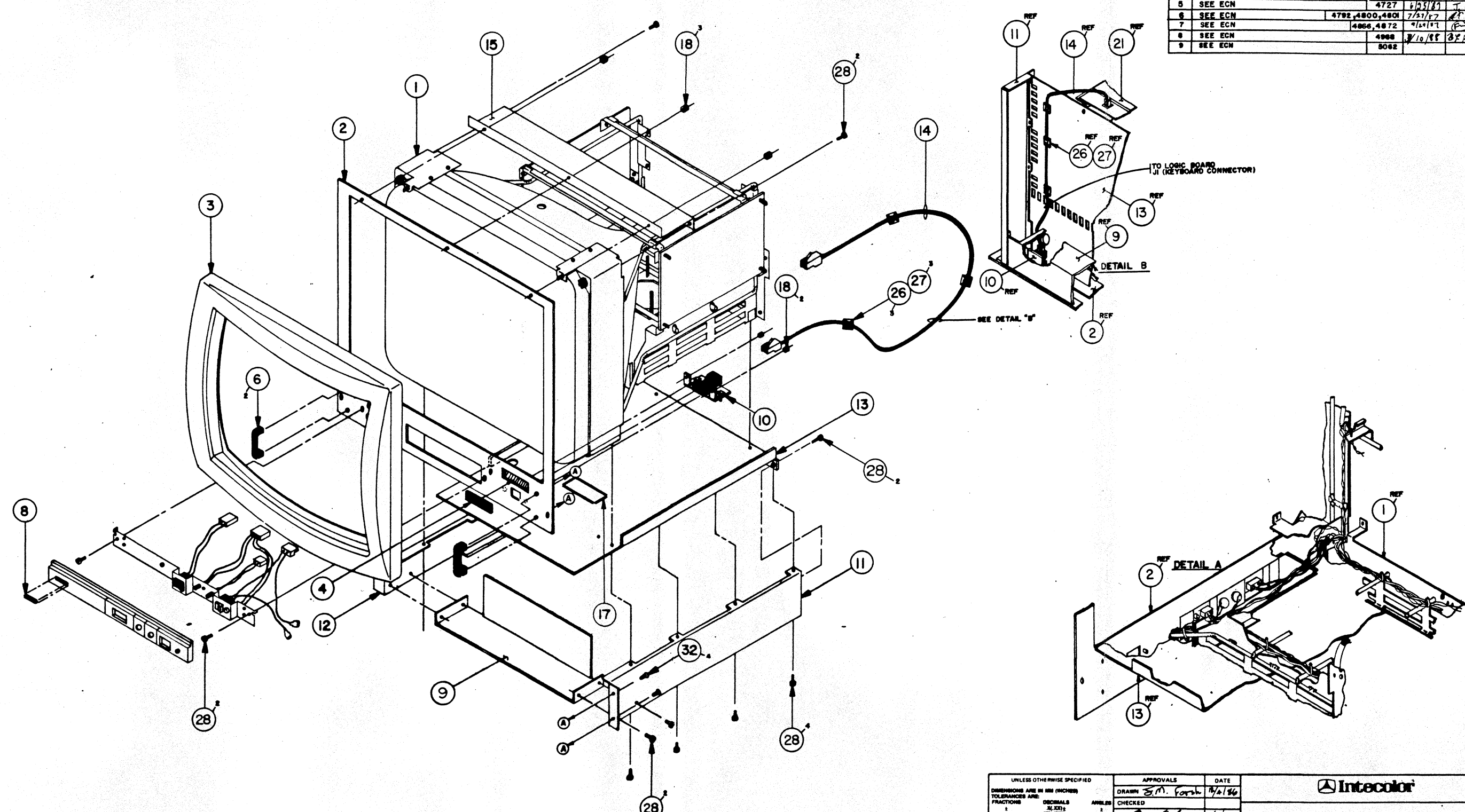


TOP ASSEMBLY
8865

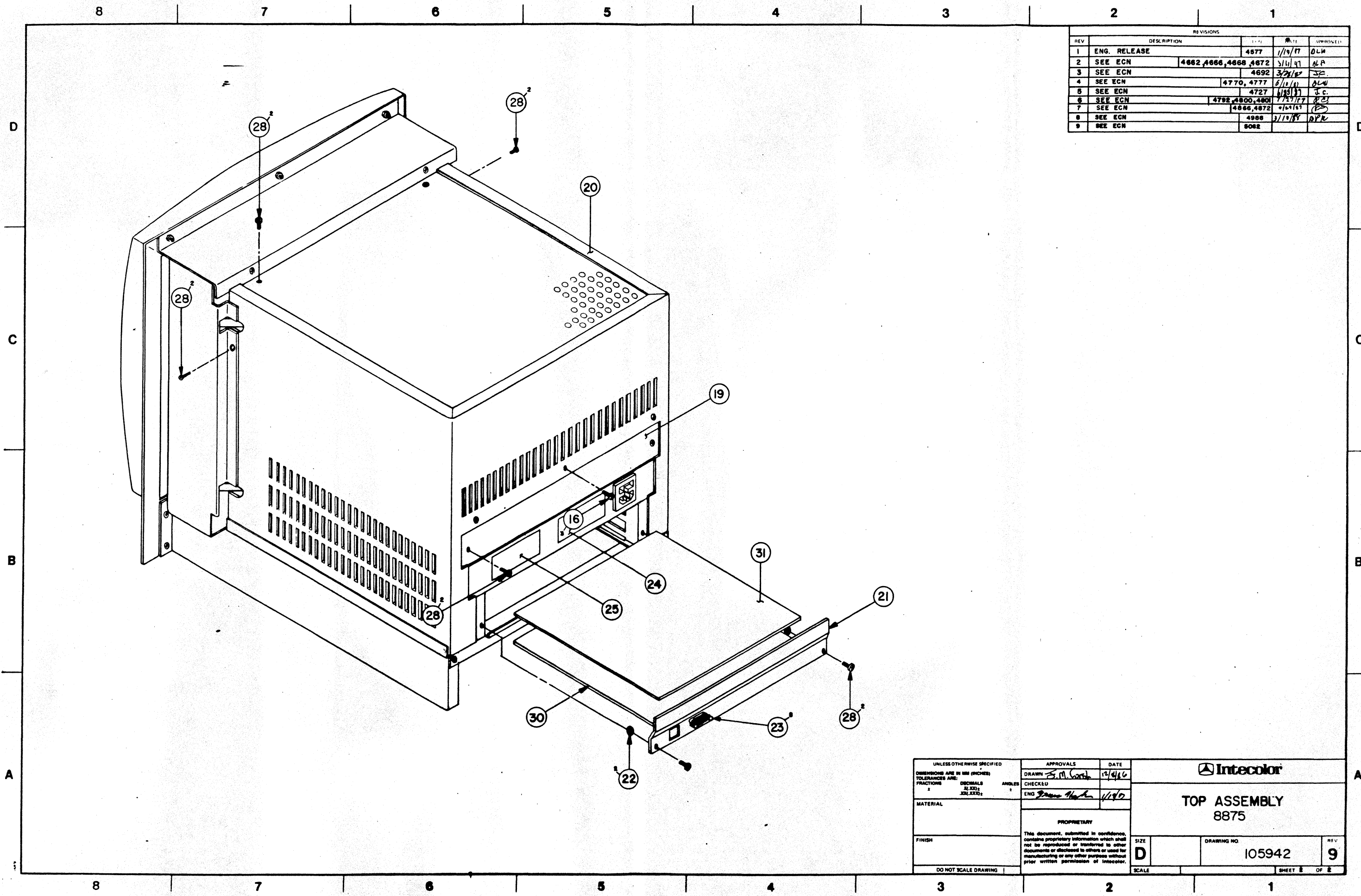
DRAWING NO. 105941
SHEET 2 OF 2

8 7 6 5 4 3 2 1

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4877	1/14/87	JLH
2	SEE ECN	4862, 4866, 4868, 4872	3/11/87	JLH
3	SEE ECN	4892	3/25/87	J.C.
4	SEE ECN	4770, 4777	6/18/87	JLH
5	SEE ECN	4727	6/23/87	J.C.
6	SEE ECN	4792, 4800, 4801	7/27/87	J.C.
7	SEE ECN	4866, 4872	9/15/87	(P)
8	SEE ECN	4988	1/10/88	B.F.H.
9	SEE ECN	5062		



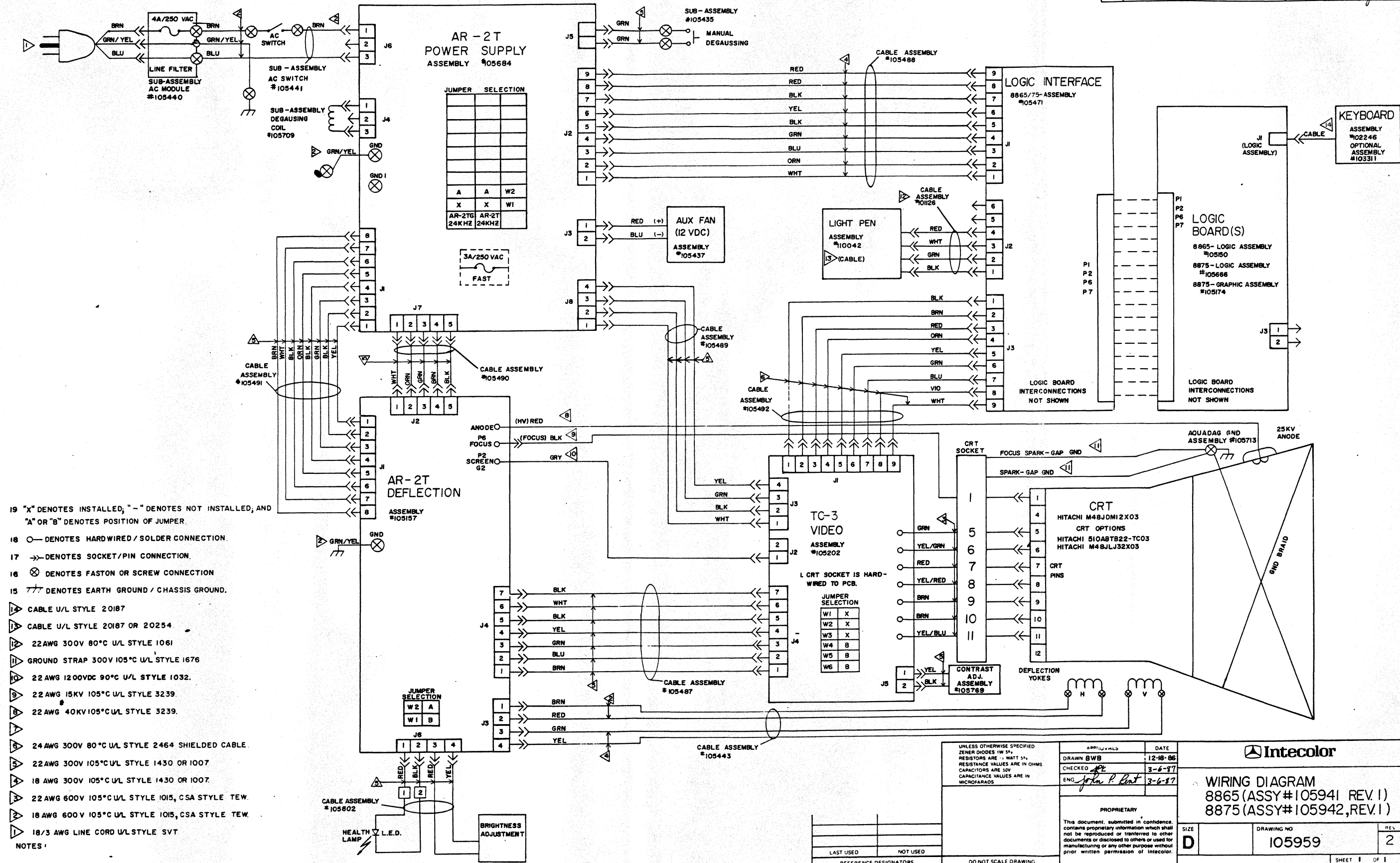
UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	 TOP ASSEMBLY 8875
DIMENSIONS ARE IN INCHES		DRAWN <i>S.M. Forth</i>		1/14/86	
TOLERANCES ARE:		CHECKED			
FRACTIONS 1/16, 1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8		ENG <i>John Nelson</i>		1/10/87	
MATERIAL		PROPRIETARY		SIZE D DRAWING NO. 105942 REV 9	
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or furnished to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SCALE 1 SHEET 1 OF 1	
DO NOT SCALE DRAWING					



REVISIONS				
REV	DESCRIPTION	DATE	BY	APPROVED
1	ENG. RELEASE	4677	1/19/77	DLW
2	SEE ECN	4662, 4666, 4668, 4672	3/16/77	ALP
3	SEE ECN	4692	3/28/77	SC
4	SEE ECN	4770, 4777	6/12/77	DLW
5	SEE ECN	4727	6/28/77	J.C.
6	SEE ECN	4782, 4800, 4801	7/27/77	J.C.
7	SEE ECN	4866, 4872	8/24/77	DLW
8	SEE ECN	4986	3/10/78	ALP
9	SEE ECN	5082		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MM (INCHES) TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .001 ± .001 ± .001		APPROVALS DRAWN <i>S.M. Galt</i> CHECKED ENG <i>John H. Hark</i>	DATE 12/4/76 1/19/77		
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		TOP ASSEMBLY 8875	
FINISH		SIZE D	DRAWING NO. 105942	REV 9	
DO NOT SCALE DRAWING		SCALE	SHEET 1 OF 2		

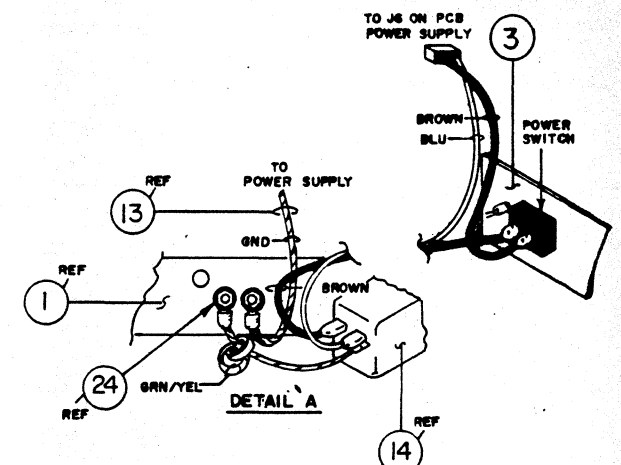
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4612	3-6-87	JPL
2	SEE ECN	4823	8-28-87	JPL



- 19 "X" DENOTES INSTALLED; "-" DENOTES NOT INSTALLED; AND "A" OR "B" DENOTES POSITION OF JUMPER.
- 18 ○ DENOTES HARDWIRED / SOLDER CONNECTION.
- 17 → DENOTES SOCKET / PIN CONNECTION.
- 16 ⊗ DENOTES FASTON OR SCREW CONNECTION.
- 15 ⚡ DENOTES EARTH GROUND / CHASSIS GROUND.
- △ CABLE U/L STYLE 20187
- △ CABLE U/L STYLE 20187 OR 20254
- △ 22AWG 300V 80°C U/L STYLE 1061
- △ GROUND STRAP 300V 105°C U/L STYLE 1676
- △ 22AWG 1200VDC 90°C U/L STYLE 1032.
- △ 22AWG 15KV 105°C U/L STYLE 3239.
- △ 22AWG 40KV 105°C U/L STYLE 3239.
- △ 24AWG 300V 80°C U/L STYLE 2464 SHIELDED CABLE.
- △ 22AWG 300V 105°C U/L STYLE 1430 OR 1007
- △ 18AWG 300V 105°C U/L STYLE 1430 OR 1007.
- △ 22AWG 600V 105°C U/L STYLE 1015, CSA STYLE TEW.
- △ 18AWG 600V 105°C U/L STYLE 1015, CSA STYLE TEW.
- △ 18/3 AWG LINE CORD U/L STYLE SVT
- NOTES:

UNLESS OTHERWISE SPECIFIED ZENER DIODES 1W 5% RESISTORS ARE 1/4 WATT 5% RESISTANCE VALUES ARE IN OHMS CAPACITORS ARE 50V CAPACITANCE VALUES ARE IN MICROFARADS		DATE 12-18-86	Intecolor	
DRAWN BWB		CHECKED JPL	WIRING DIAGRAM	
ENG. JPL		DATE 3-6-87	8865 (ASSY#105941 REV.1)	
PROPRIETARY		8875 (ASSY#105942, REV.1)		
This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SIZE D	DRAWING NO 105959	REV 2
LAST USED		DO NOT SCALE DRAWING		SHEET 1 OF 1
REFERENCE DESIGNATORS				

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4656	3/11/97	GLW
2	SEE ECN	4702	7/22/97	GLW
3	SEE ECN	4773	6/12/97	GLW
4	SEE ECN	4823, 4935	5-28-97	JPE
5	SEE ECN	4914, 4915	1/20/98	J.C.
6	SEE ECN	4998	3-10-98	J.C.
7	SEE ECN	5025, 5031	5-19-98	SK

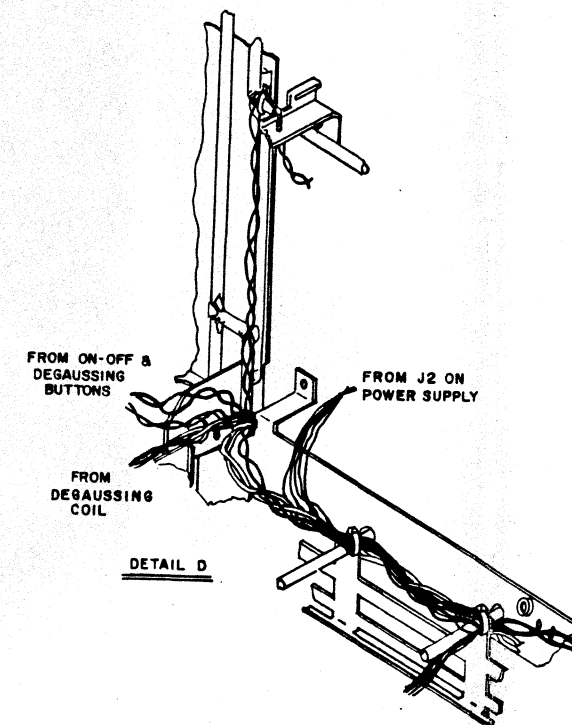
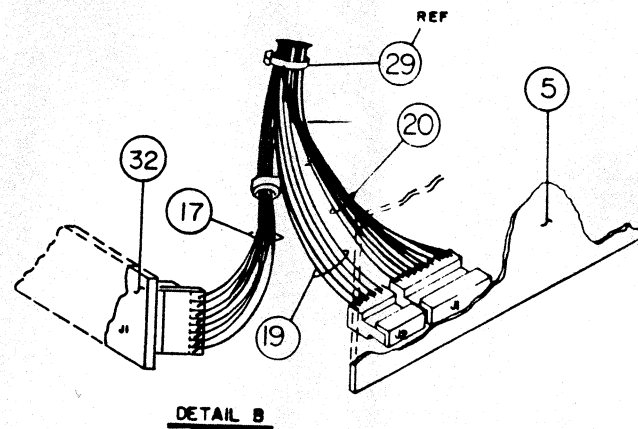


NOTES:

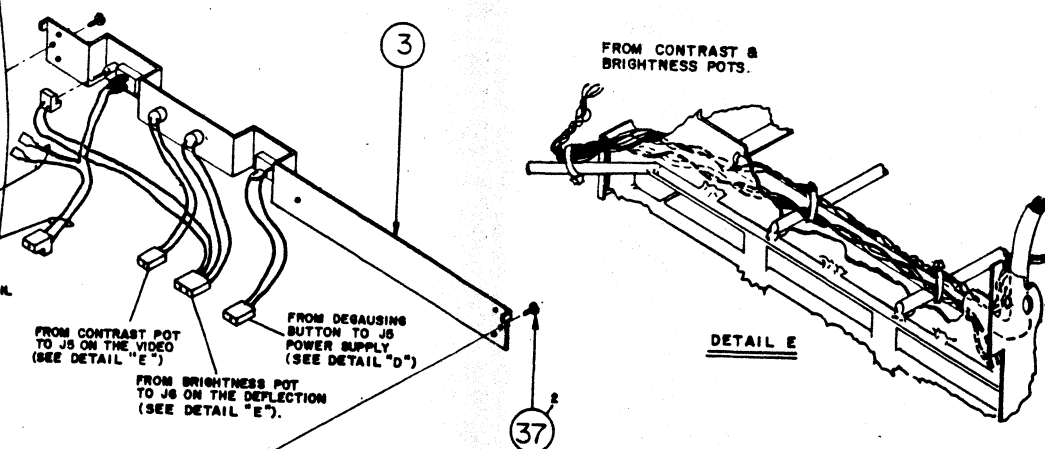
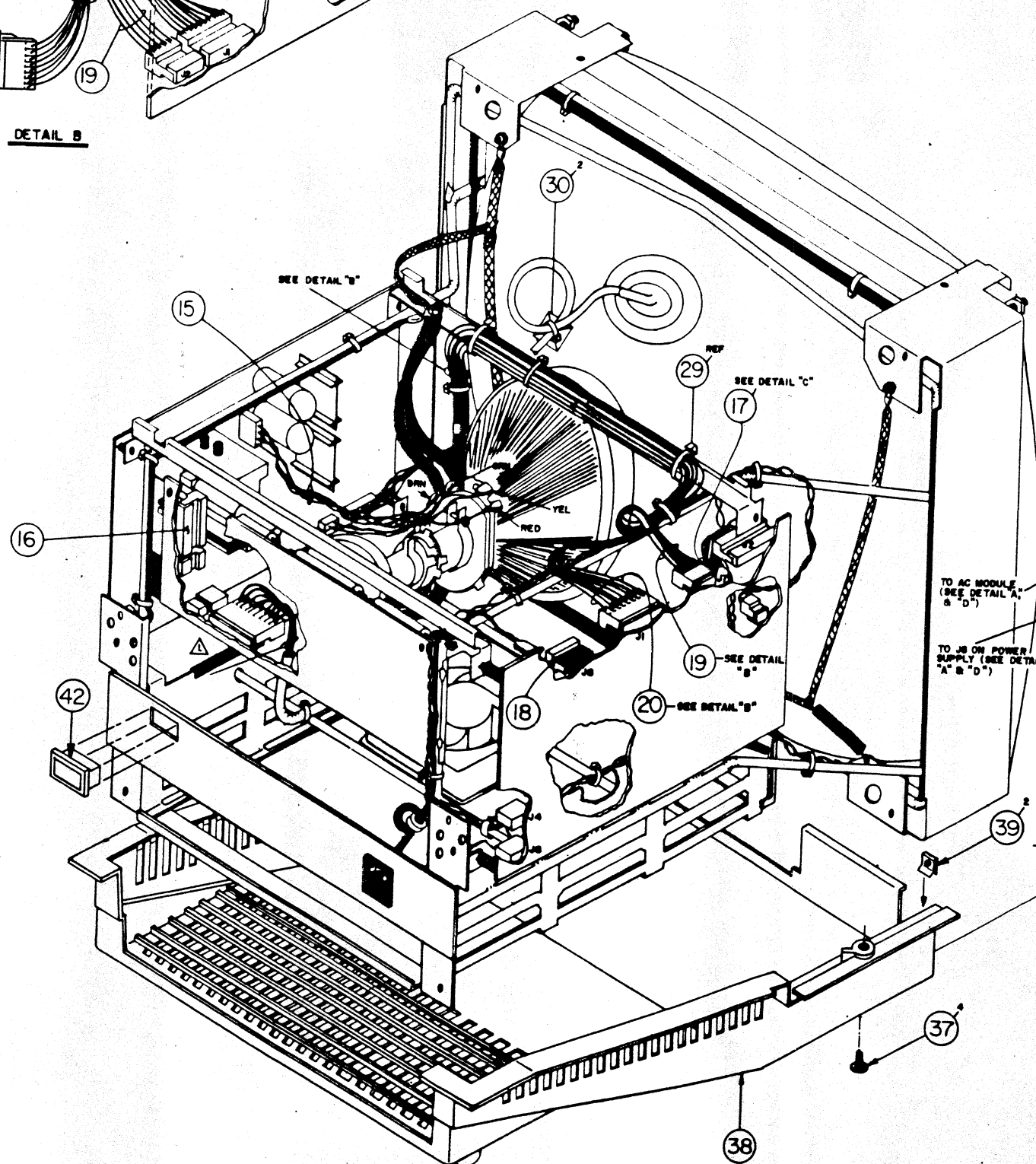
⚠ COVER EDGE OF METAL WITH CATERPILLAR GROMMET
ITEM 27.

⚠ UNIT MUST BE BURNED IN, TESTED, AND SHIPPED WITH
THE SAME LINE COND.

ALL DIMENSIONS UNLESS SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES FIRST SECOND THIRD XXX		APPROVALS DRAWN BWB CHECKED ENG Bruce Rogers 3/1/87		DATE 2-13-87	
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intelligent Systems			
FINISH		SIZE D		DRAWING NO 105964	
DO NOT SCALE DRAWING		SCALE		REV 7	
				SHEET 1 OF 2	

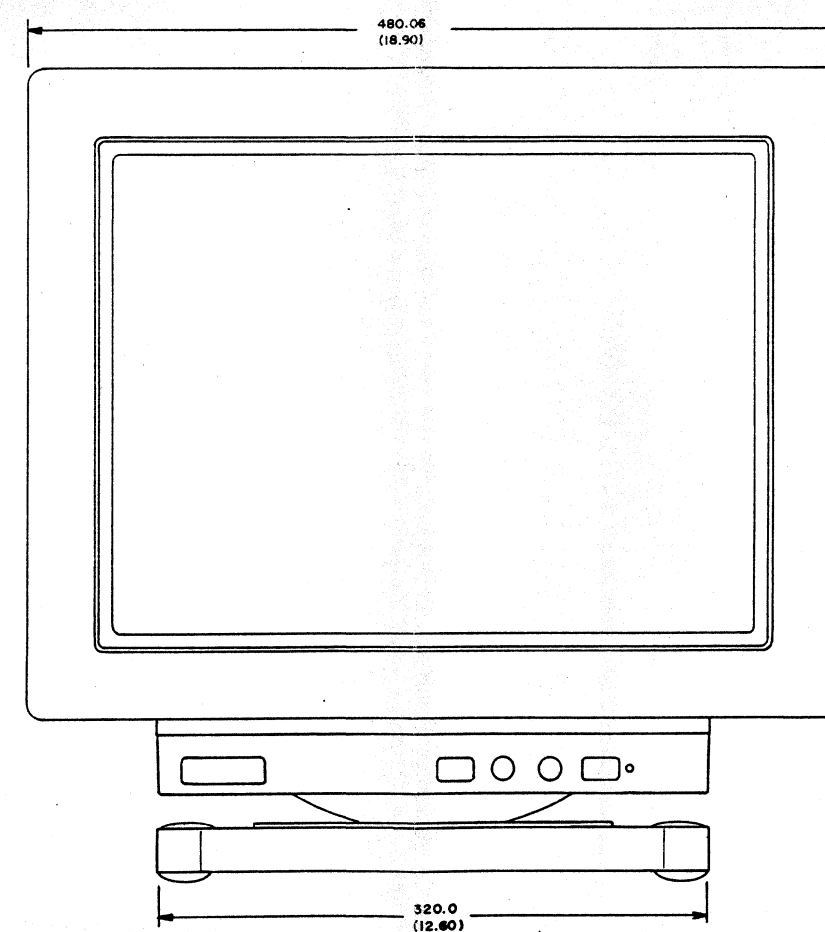
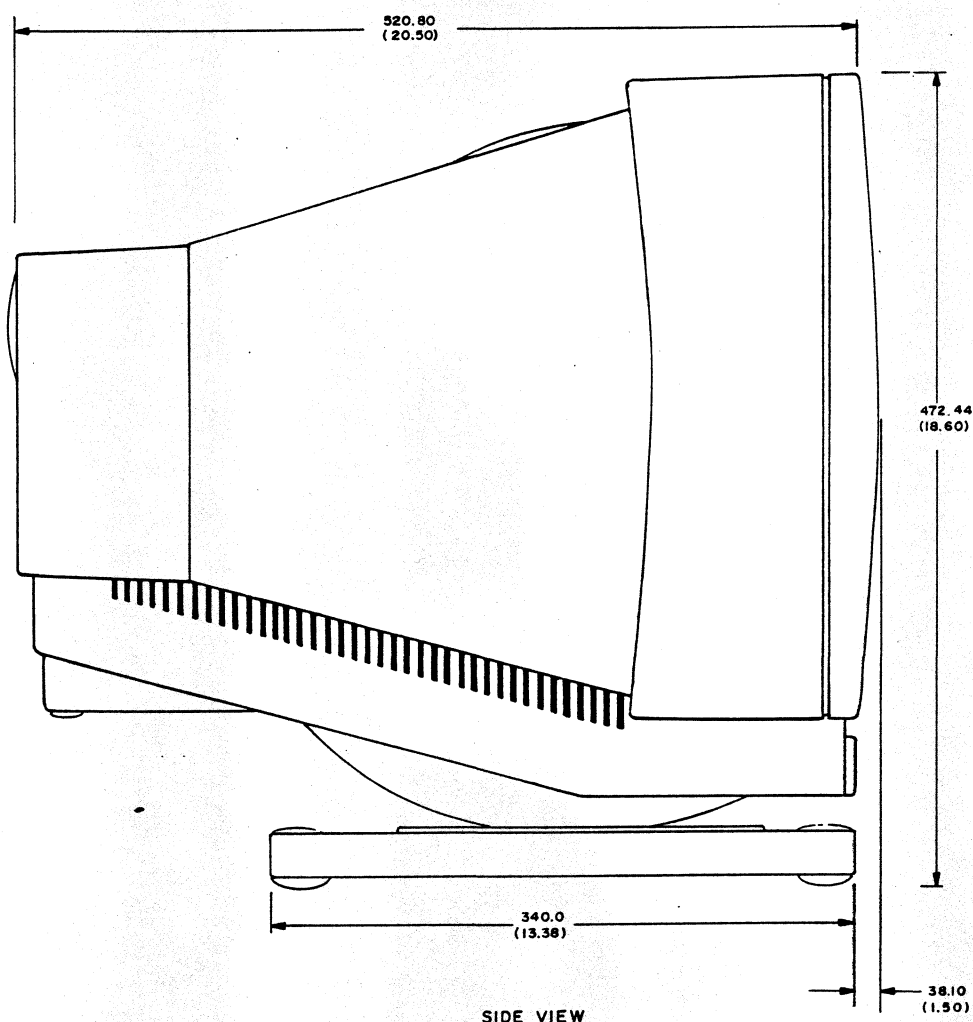


REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	4696	3/17/87	SLP
2	SEE ECN	4702	3/11/87	SLP
3	SEE ECN	4773	6/12/87	SLP
4	SEE ECN	4823/4835	8-28-87	APC
5	SEE ECN	4914, 4916	1/26/88	J.C.
6	SEE ECN	4998	5-18-88	YDK
7	SEE ECN	5025, 5031	5-17-88	J.C.



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE
DIMENSIONS ARE IN INCHES FRACTIONS ARE		DESIGNED BY	CHECKED	2-15-87
DECIMALS ARE		ENG. <i>Bruce Taylor</i>		3/17/87
MATERIAL		PROPRIETARY		
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		
DO NOT SCALE DRAWING				
		CHASSIS ASSEMBLY CMR-2 FRONT CONTROL		
		SIZE	DRAWING NO.	REV
		D	105964	7
		SCALE	SHEET 2 OF 2	

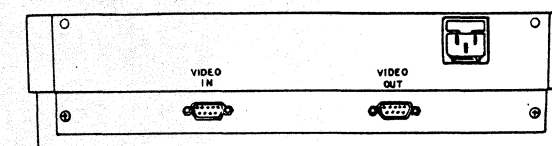
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4729	5/18/87	RLB



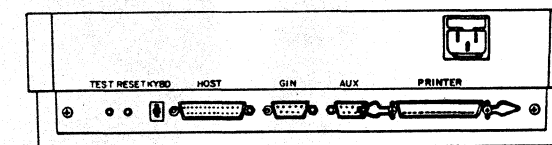
UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	 ENVELOPE DRAWING ERGONOMICS CASE EGA MONITOR, C42 SERIES LOGIC 8800 SERIES LOGIC
DIMENSIONS ARE IN MM (INCHES)		DRAWN BWB		4-3-87	
TOLERANCES ARE:		CHECKED			
FRACTIONS		ENG <i>[Signature]</i>		5/19/87	
MATERIAL		PROPRIETARY		SIZE D DRAWING NO. 105985 REV 1	
FINISH		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		SCALE SHEET 1 OF 2	
DO NOT SCALE DRAWING					

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4729	5/18/87	OLM

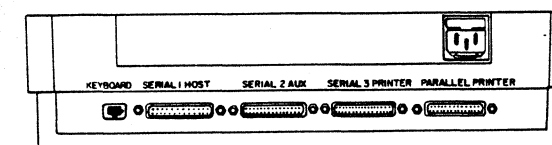
CONNECTOR PLATE CONFIGURATIONS



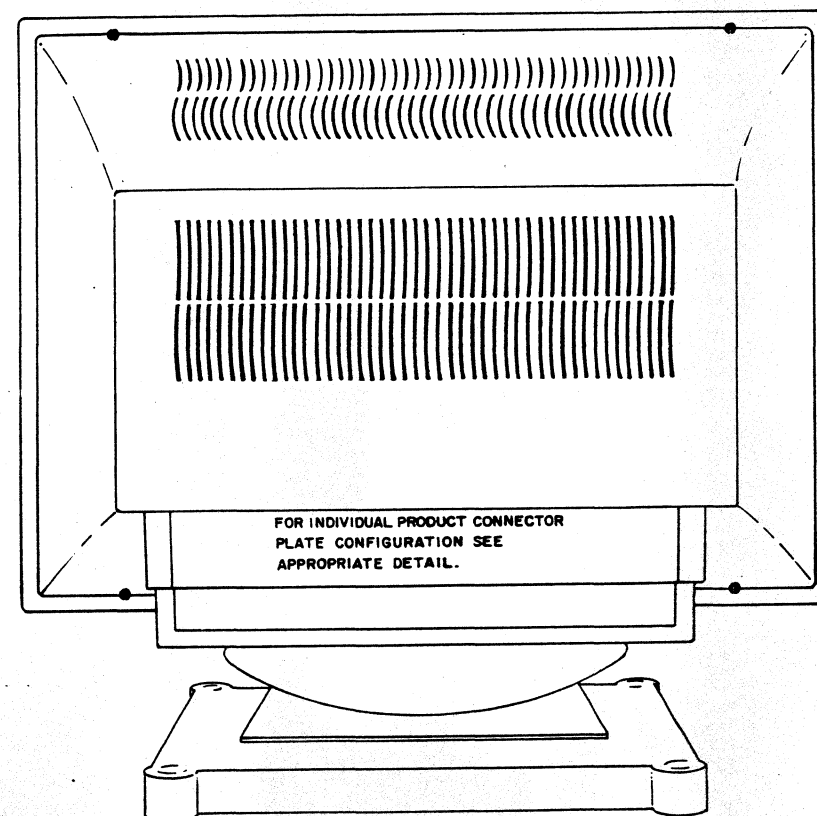
EGA MONITOR



C42 SERIES LOGIC



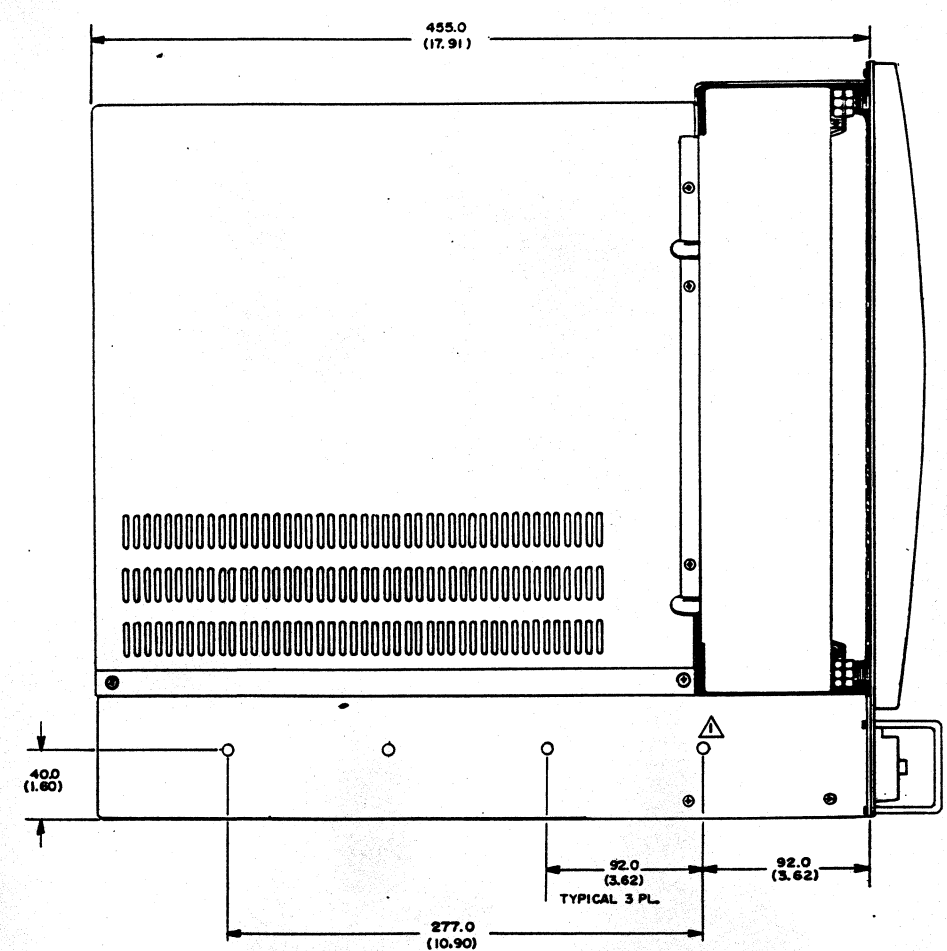
8800 SERIES LOGIC



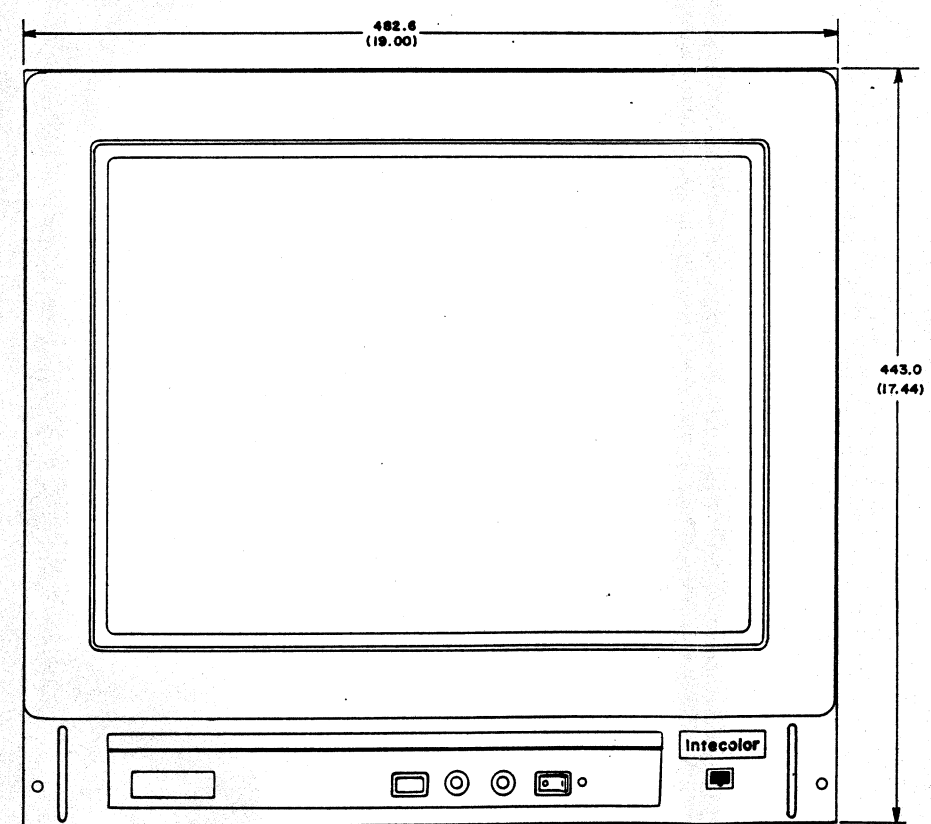
REAR VIEW

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	Intecolor	
DIMENSIONS ARE IN MM (INCHES)		DRAWN BWB		4-3-87	ENVELOPE DRAWING ERGONOMICS CASE EGA MONITOR, C42 SERIES LOGIC 8800 SERIES LOGIC	
TOLERANCES ARE:		CHECKED				
FRACTIONS		ENG <i>Steve High</i>		5/18/87		
MATERIAL		PROPRIETARY		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		
FINISH		SIZE		D	DRAWING NO. 105985	
DO NOT SCALE DRAWING		SCALE		SHEET 2 OF 2		

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4729	5/18/87	BZM
2	SEE ECN	4936	2/8/88	BZM
3	SEE ECN	5048	6/1/88	BZM

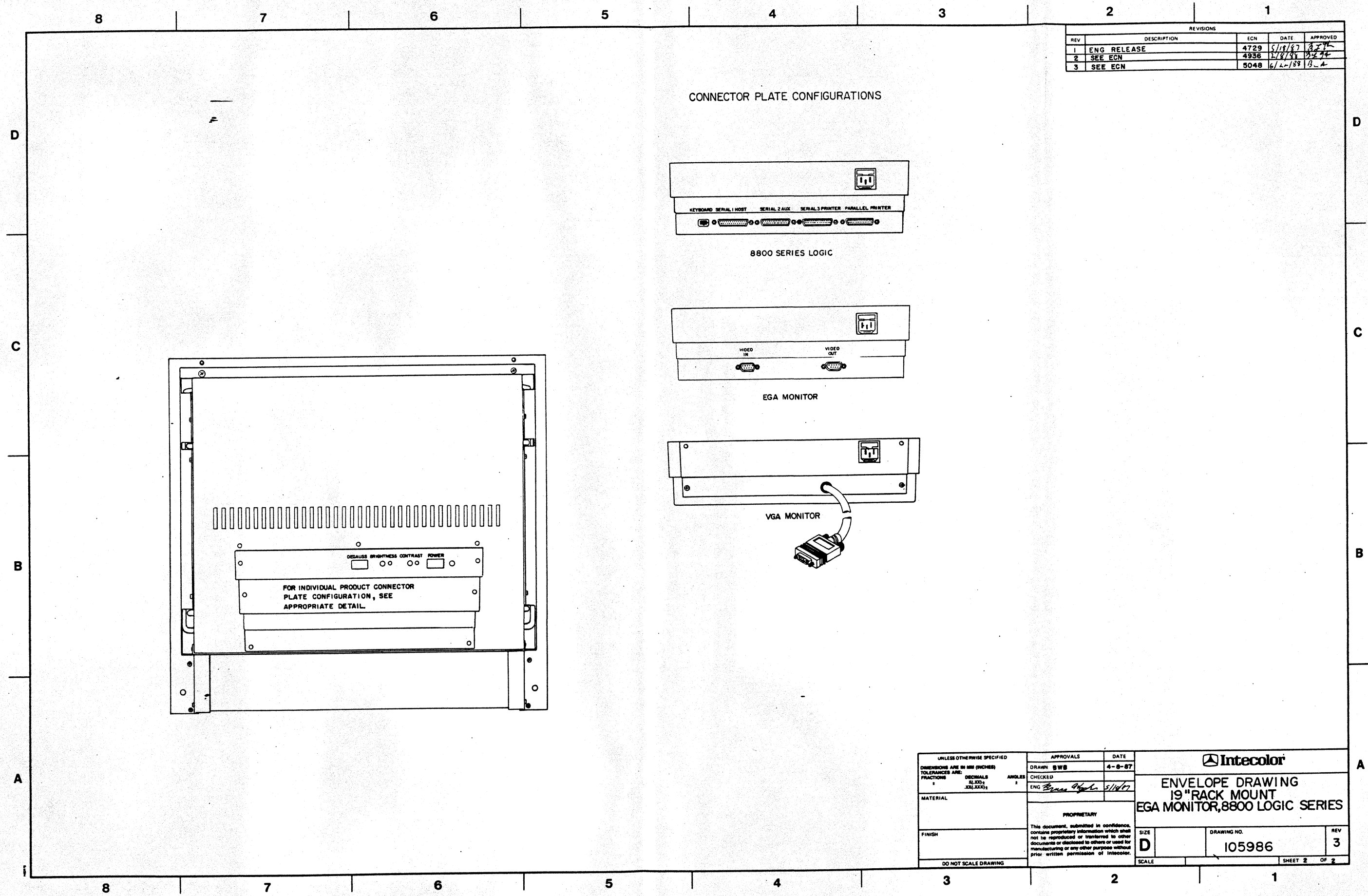


NOTES:
 △ HOLE SPACING FOR CHASSIS-TRAK C-300-S SLIDES



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE
DIMENSIONS ARE IN MM (INCHES)		DRAWN BWS		4-8-87
TOLERANCES ARE:		CHECKED		
FRACTIONS	DECIMALS	ENG <i>[Signature]</i>		5/18/87
1	0.125			
2	0.250			
MATERIAL		PROPRIETARY		
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DO NOT SCALE DRAWING				

Intecolor		
ENVELOPE DRAWING 19" RACK MOUNT EGA MONITOR, 8800 LOGIC SERIES		
SIZE D	DRAWING NO. 105986	REV 3
SCALE		SHEET 1 OF 2



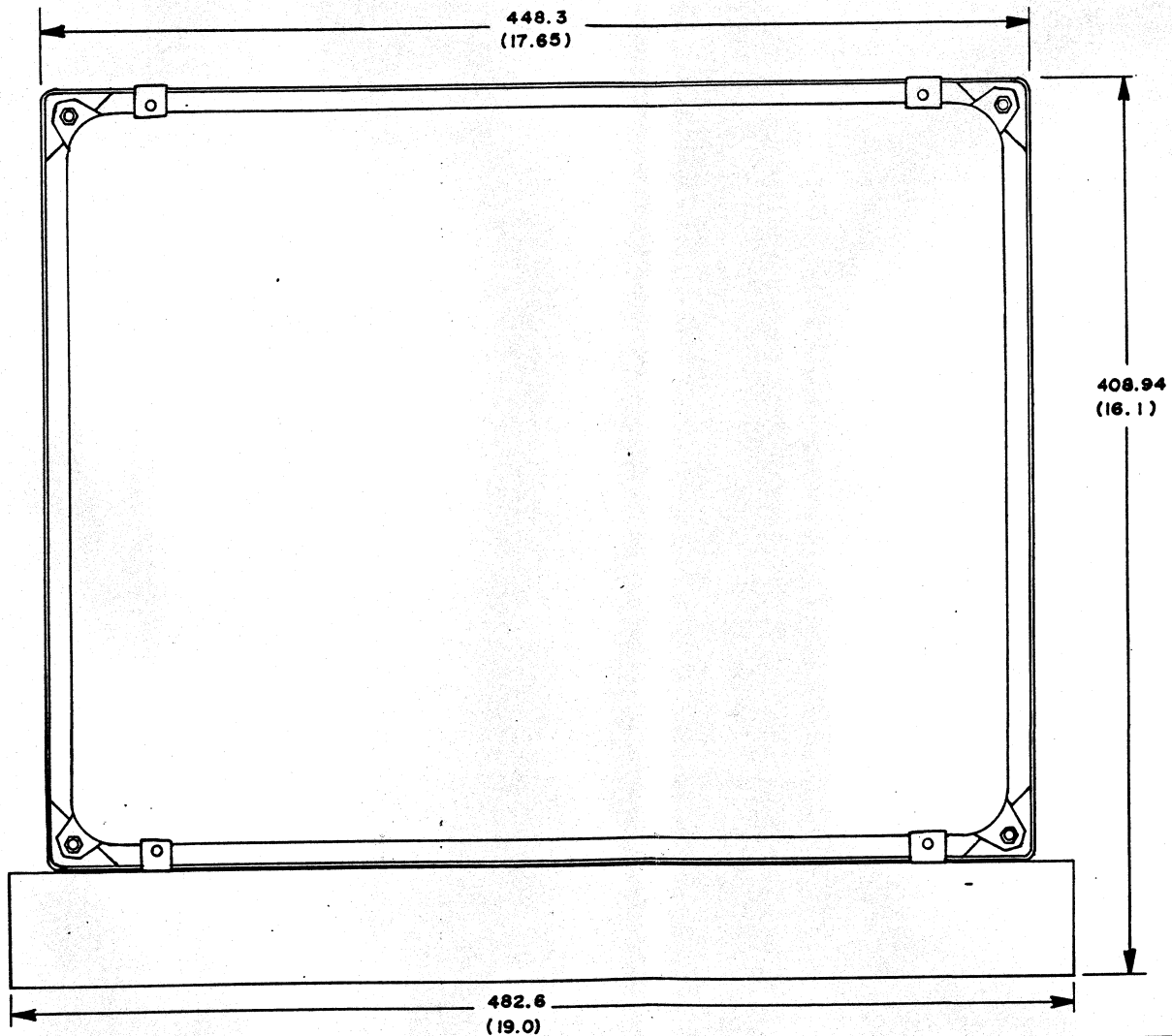
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	4729	5/18/87	B-4
2	SEE ECN	4936	2/8/88	B-4
3	SEE ECN	5048	6/22/88	B-4

UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE		
DIMENSIONS ARE IN INCHES (RACHES)		DRAWN BWS		4-8-87		
TOLERANCES ARE:		CHECKED				
FRACTIONS	DECIMALS	ENG <i>Bruce Ogden</i>		5/18/87		
1/16	.0005					
1/32	.0010					
1/64	.0020					
MATERIAL	PROPRIETARY					
FINISH	This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.					
DO NOT SCALE DRAWING		SIZE	DRAWING NO.	REV		
		D	105986	3		
		SCALE	SHEET 2 OF 2			



ENVELOPE DRAWING
19" RACK MOUNT
EGA MONITOR, 8800 LOGIC SERIES

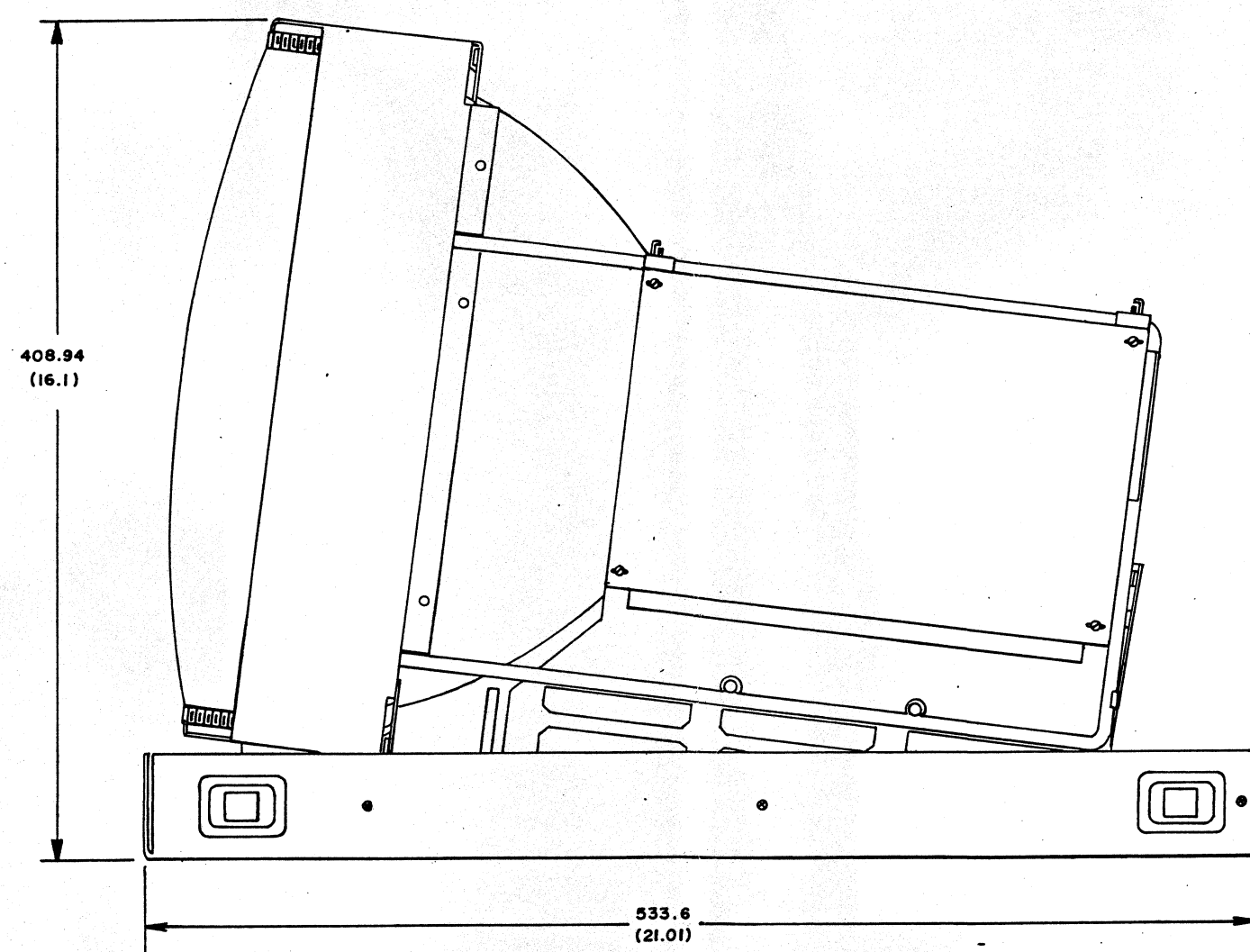
REVISIONS				
REV	DESCRIPTION	ECN	APPROVED	DATE
1	ENG RELEASE	4729	BLH	5/18/87



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE
DIMENSIONS ARE IN MM (INCHES)		DRAWN <i>BWB</i>		5/18/86
TOLERANCES ARE:		CHECKED		
FRACTIONS	DECIMALS	ENG <i>[Signature]</i>		5/18/87
±	.X(.XX)± .XX(.XXX)±			
ANGLES		PROPRIETARY		
±		This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.		
MATERIAL				
FINISH				
DO NOT SCALE DRAWING				

ENVELOPE DRAWING 19" CONSOLE FRONT VIEW			
SIZE	DRAWING NO.	REV	
C	105987	1	
SCALE	SHEET 1 OF 2		

REVISIONS				
REV	DESCRIPTION	ECN	APPROVED	DATE
1	ENG RELEASE	4729	<i>BJK</i>	5/18/87



UNLESS OTHERWISE SPECIFIED		APPROVALS		DATE	
DIMENSIONS ARE IN MM (INCHES)		DRAWN <i>BWB</i>	12/18/86		
TOLERANCES ARE:		CHECKED			
FRACTIONS	DECIMALS	ANGLES	ENG <i>James Adelman</i>	5/18/87	
±	.XX(.XX)±	±			
MATERIAL		PROPRIETARY This document, submitted in confidence, contains proprietary information which shall not be reproduced or transferred to other documents or disclosed to others or used for manufacturing or any other purpose without prior written permission of Intecolor.			
FINISH		SIZE C DRAWING NO. 105987 REV 1			
DO NOT SCALE DRAWING		SCALE SHEET 2 OF 2			

ENVELOPE DRAWING
19" CONSOLE
SIDE VIEW